# Computer Organization and Architecture

Under Graduate Course
(B. Tech-Information Technology, 2nd Semester)
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By


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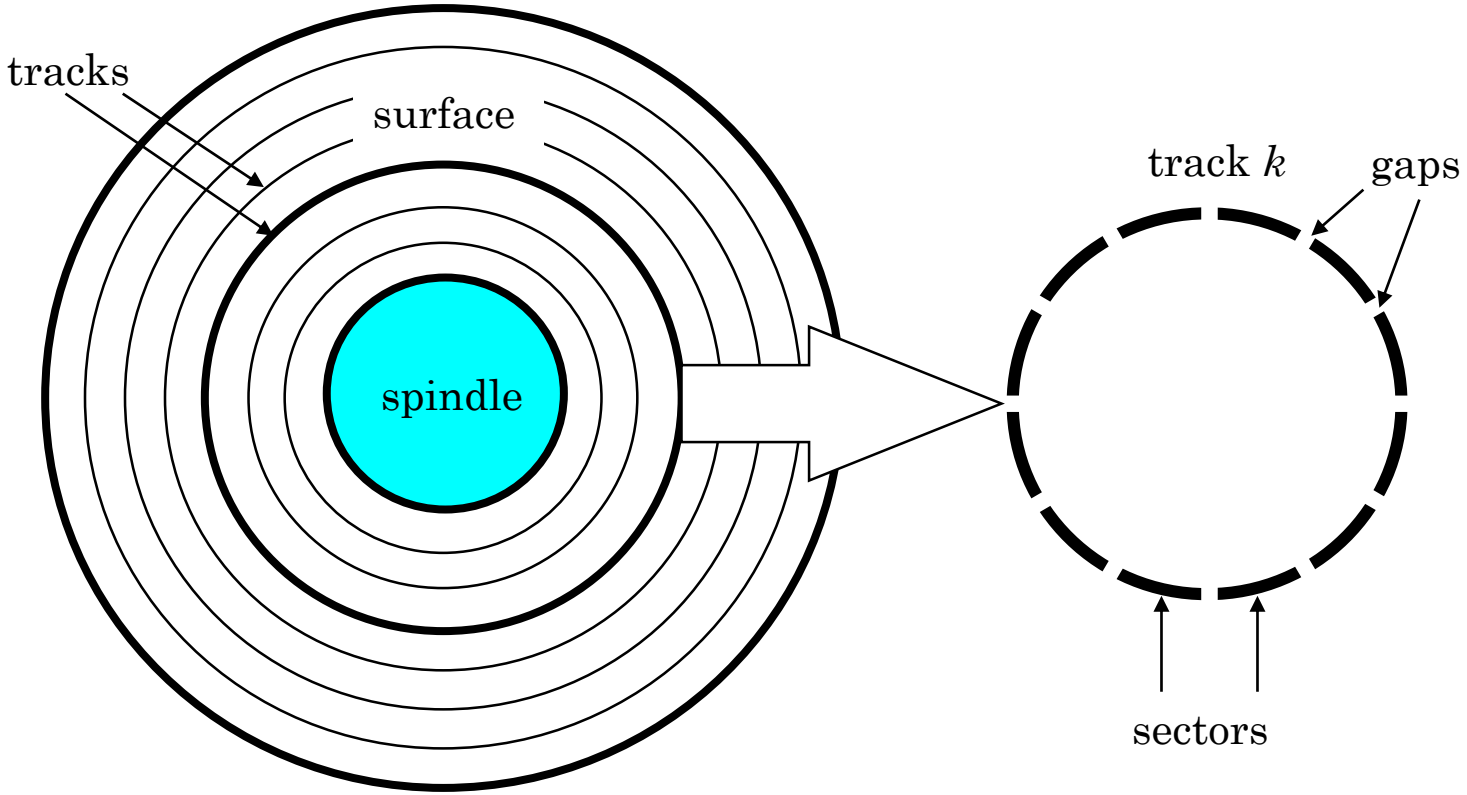
# Secondary memory and IO

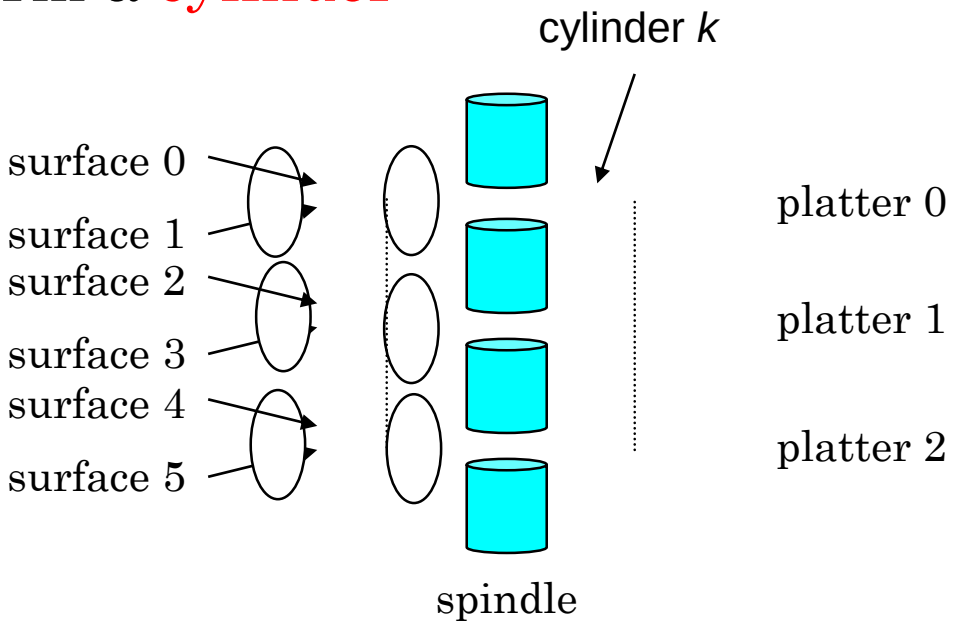
# Disk Geometry

- Disks consist of platters, each with two surfaces
- Each surface consists of concentric rings called tracks
- Each track consists of sectors separated by gaps

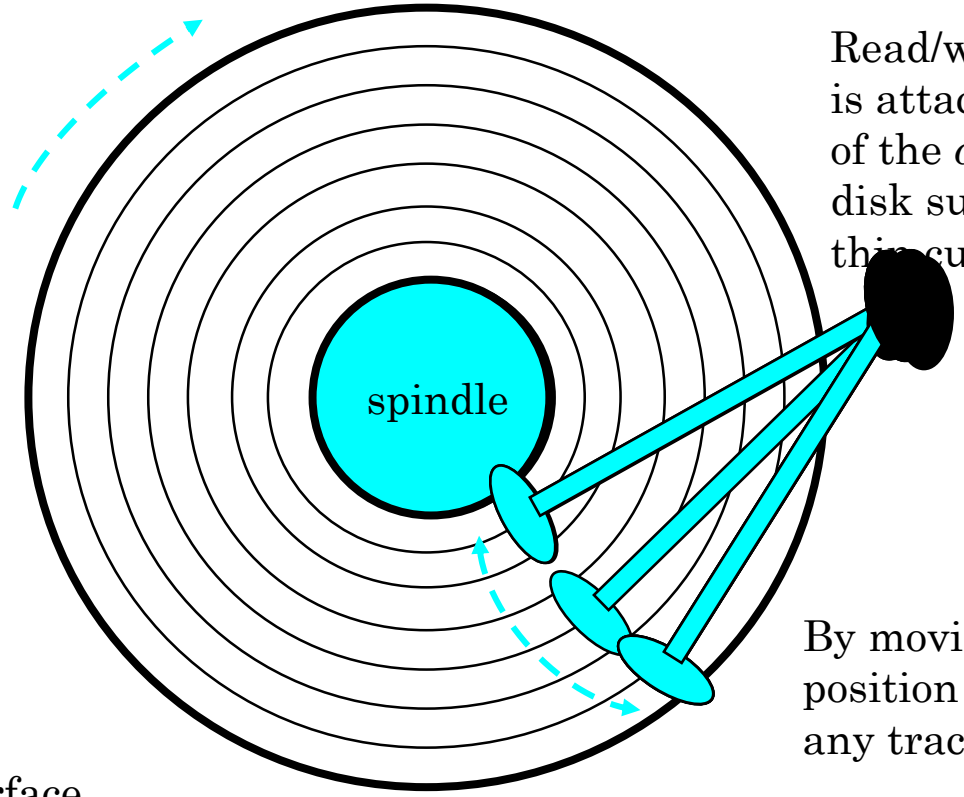


# Disk Geometry (Muliple-Platter View)

- Aligned tracks form a cylinder



# Disk Operation (Single-Platter View)

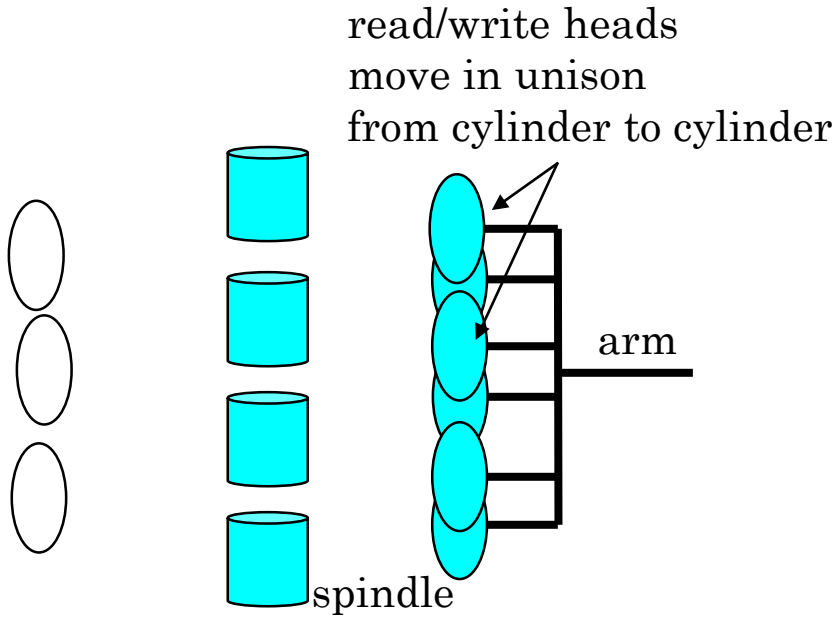



Read/write *head* is attached to end of the *arm* and flies over disk surface on thin cushion of air

By moving radially, arm can position read/write head over any track

The disk surface spins at a fixed rotational rate

# Disk Operation (Multi-Platter View)



# Disk Access Time

- Average time to access some target sector approximated by
  - Taccess = Tavg seek + Tavg rotation + Tavg transfer
- Seek time (Tavg seek)
  - Time to position heads over cylinder containing target sector
  - Typical Tavg seek = 9 ms
- Rotational latency (Tavg rotation)
  - Time waiting for first bit of target sector to pass under r/w head
  - Tavg rotation = 1/2 x 1/RPMs x 60 sec/1 min
- Transfer time (Tavg transfer)
  - Time to read the bits in the target sector.
  - Tavg transfer = 1/RPM x 1/(avg # sectors/track) x 60 secs/1 min

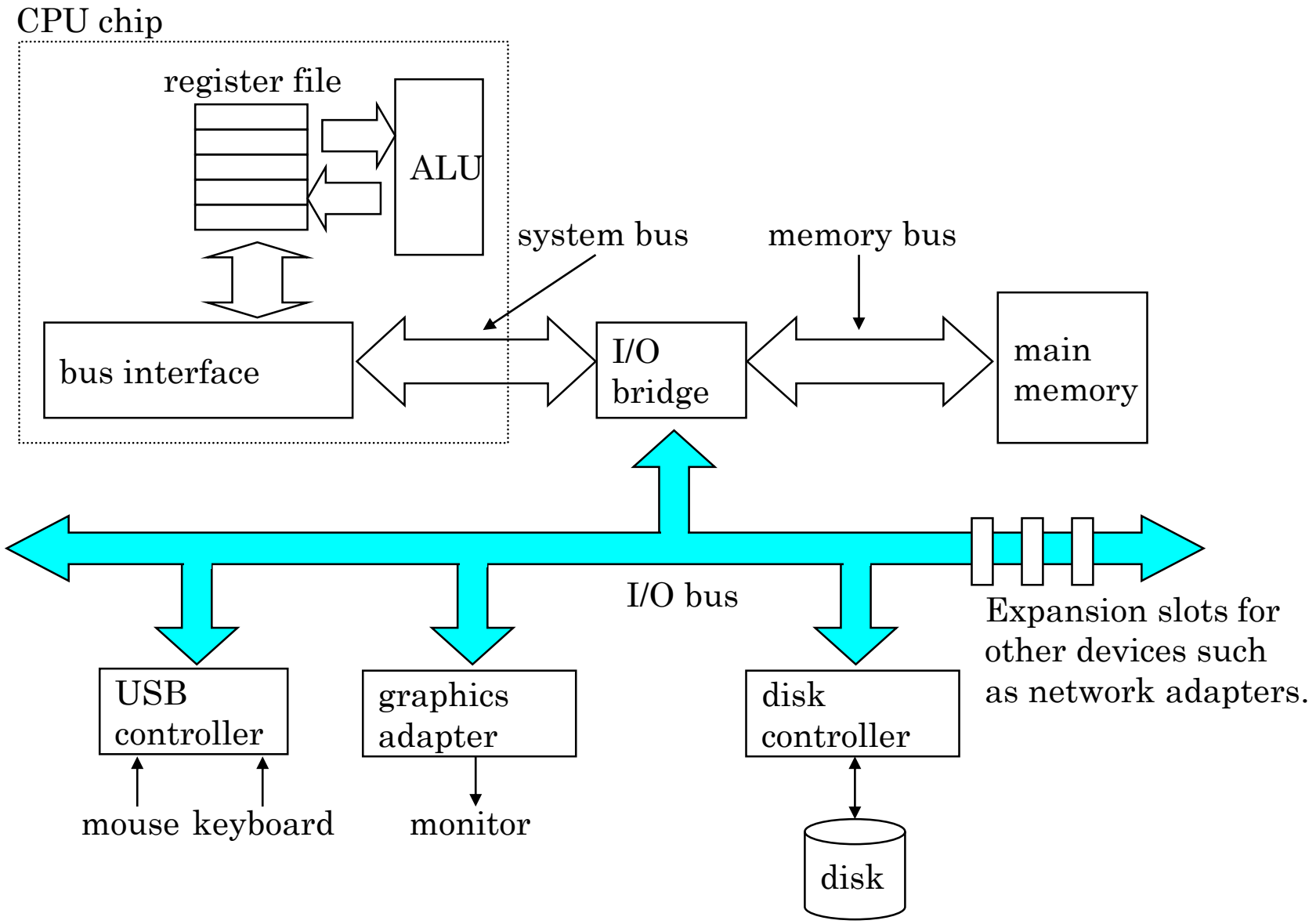
# Disk Access Time Example

- Given:
  - Rotational rate = 7,200 RPM
  - Average seek time = 9 ms
  - Avg # sectors/track = 400
- Derived:
  - Tavg rotation = 1/2 x (60 secs/7200 RPM) x 1000 ms/sec = 4 ms
  - Tavg transfer = 60/7200 RPM x 1/400 secs/track x 1000 ms/sec = 0.02 ms
  - Taccess = 9 ms + 4 ms + 0.02 ms
- Important points:
  - Access time dominated by seek time and rotational latency
  - First bit in a sector is the most expensive, the rest are free
  - SRAM access time is about 4 ns/doubleword, DRAM about 60 ns
    - Disk is about 40,000 times slower than SRAM, and
    - 2,500 times slower then DRAM

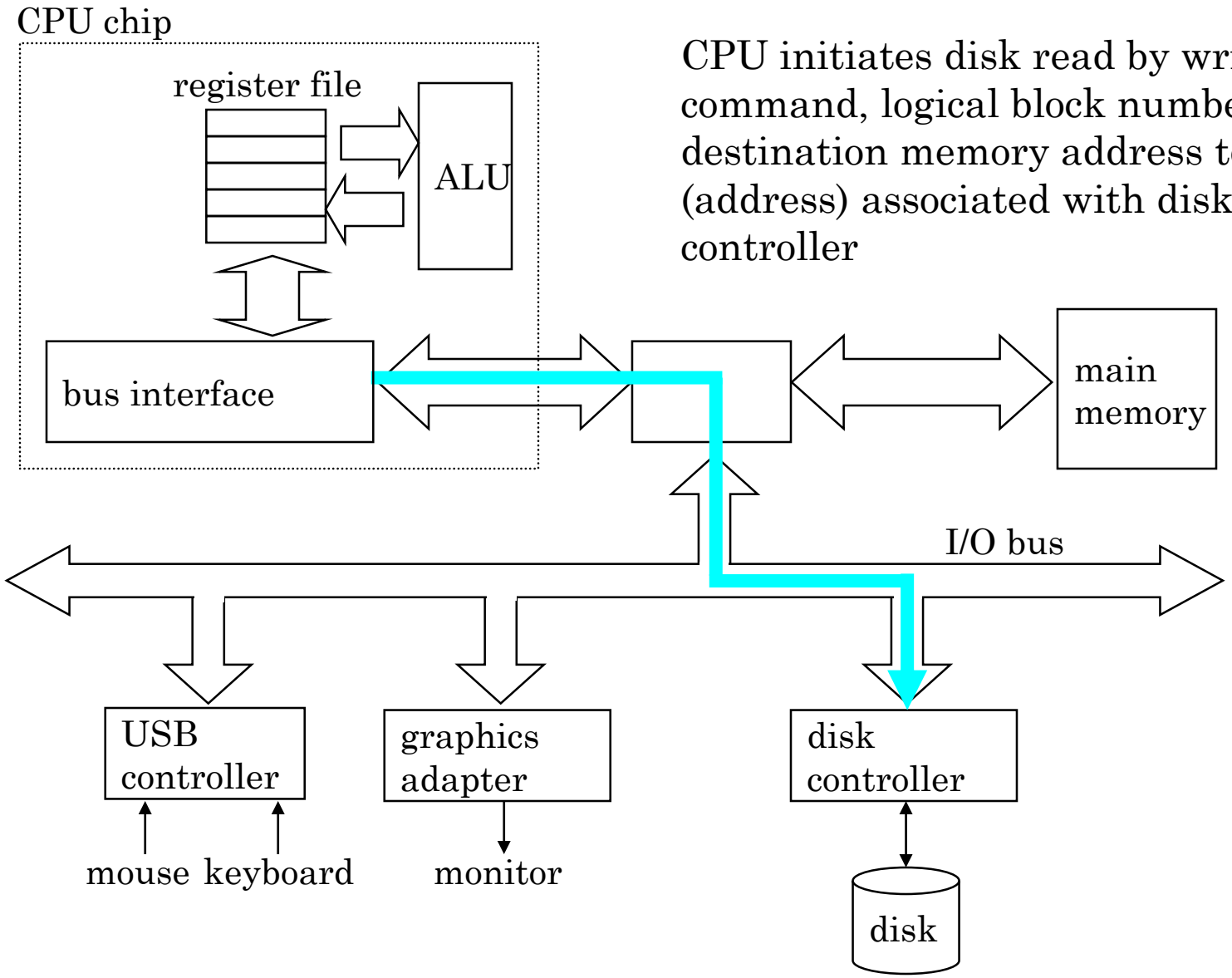
# Logical Disk Blocks

- Modern disks present a simpler abstract view of the complex sector geometry:
  - The set of available sectors is modeled as a sequence of b-sized logical blocks (0, 1, 2, ...)
- Mapping between logical blocks and actual (physical) sectors
  - Maintained by hardware/firmware device called *disk controller*
  - Converts requests for logical blocks into (surface,track,sector) triples
- Allows controller to set-aside spare cylinders for each zone
  - Accounts for the difference in "formatted capacity" and "maximum capacity"

# I/O Bus

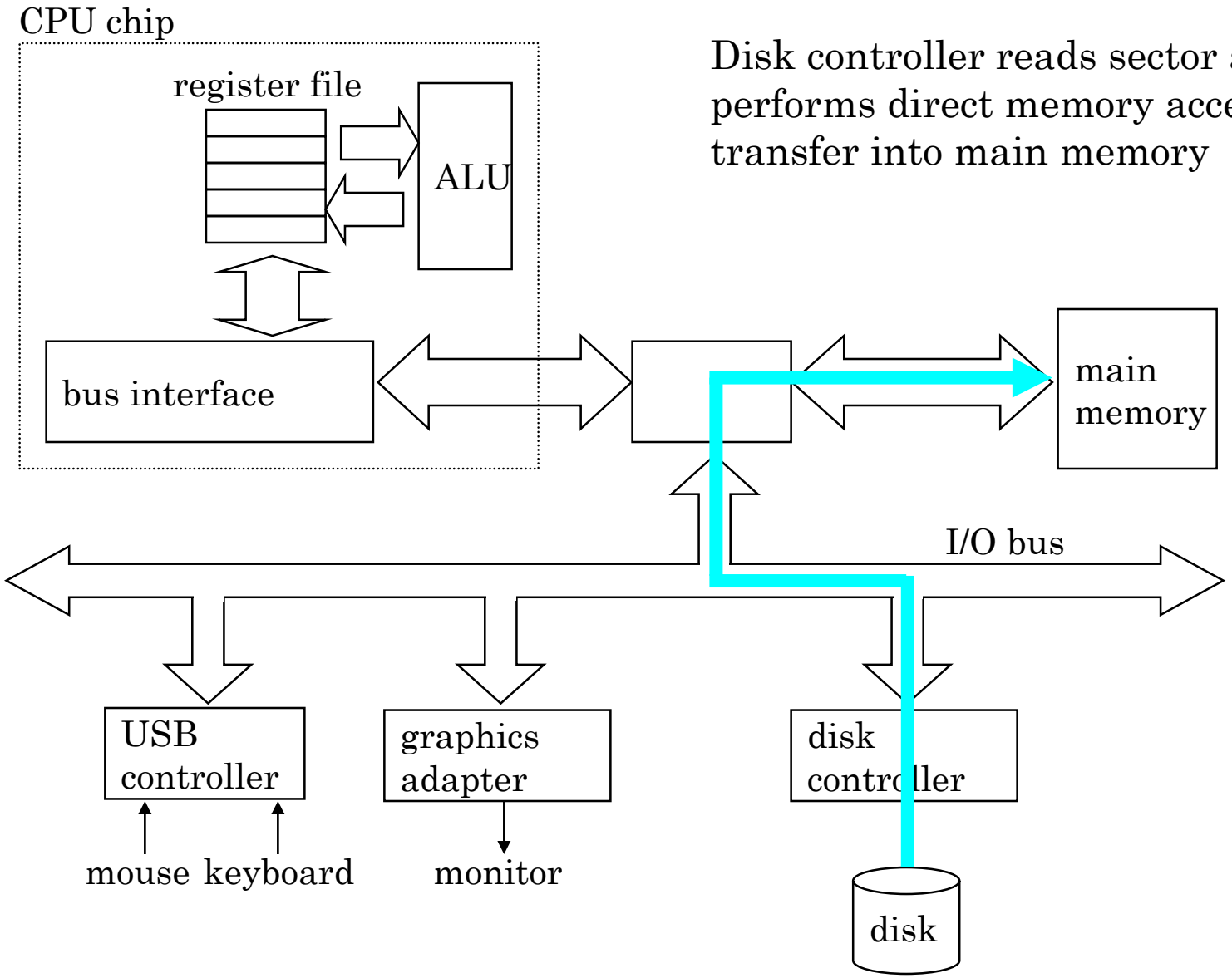

CPU chip
register file
ALU
system bus
memory bus
bus interface
I/O bridge
main memory
I/O bus
Expansion slots for other devices such as network adapters.
USB controller
graphics adapter
disk controller
mouse
keyboard
monitor
disk

# Reading a Disk Sector (1)



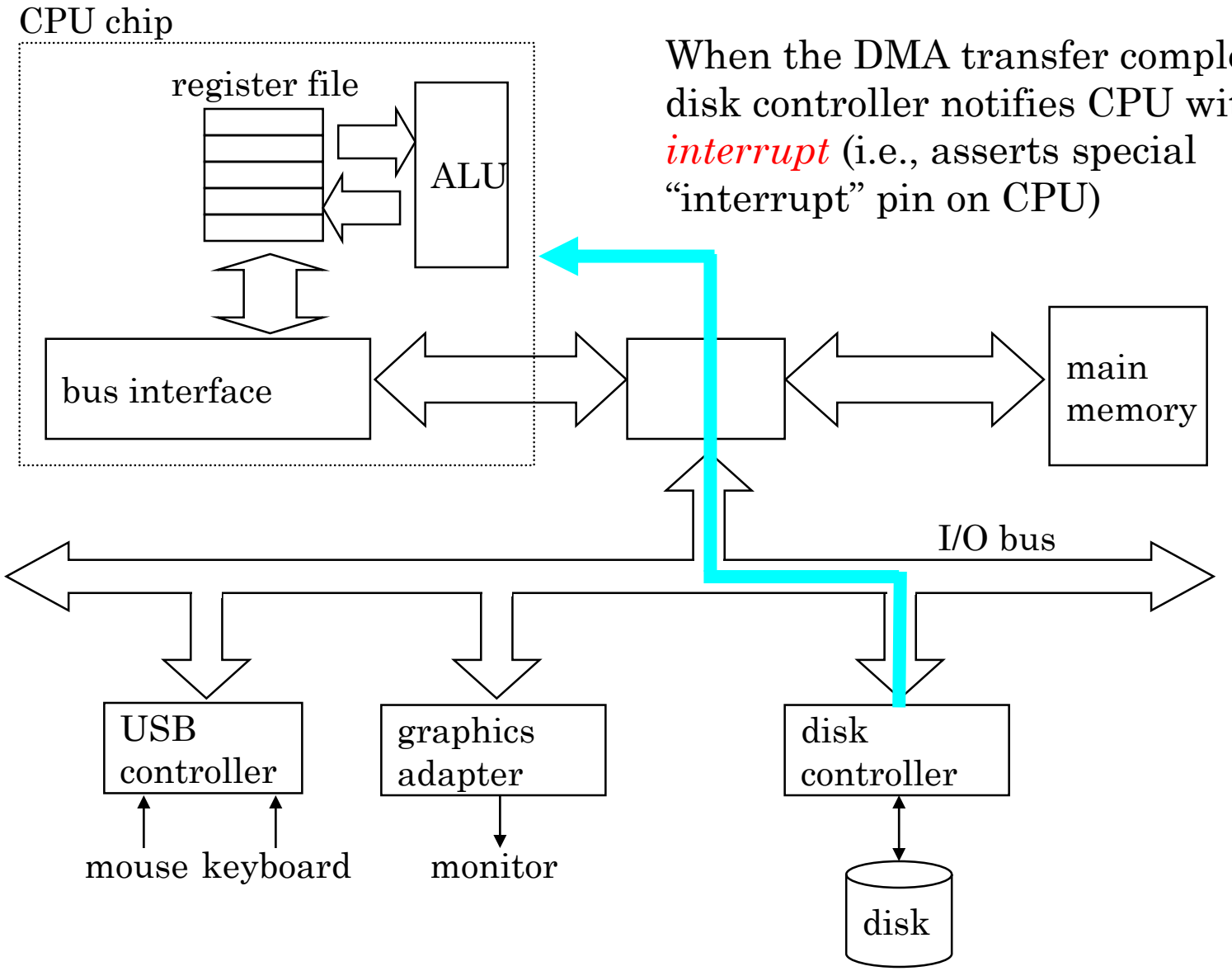

CPU initiates disk read by writing command, logical block number, and destination memory address to a port (address) associated with disk controller

# Reading a Disk Sector (2)




Disk controller reads sector and performs direct memory access (DMA) transfer into main memory

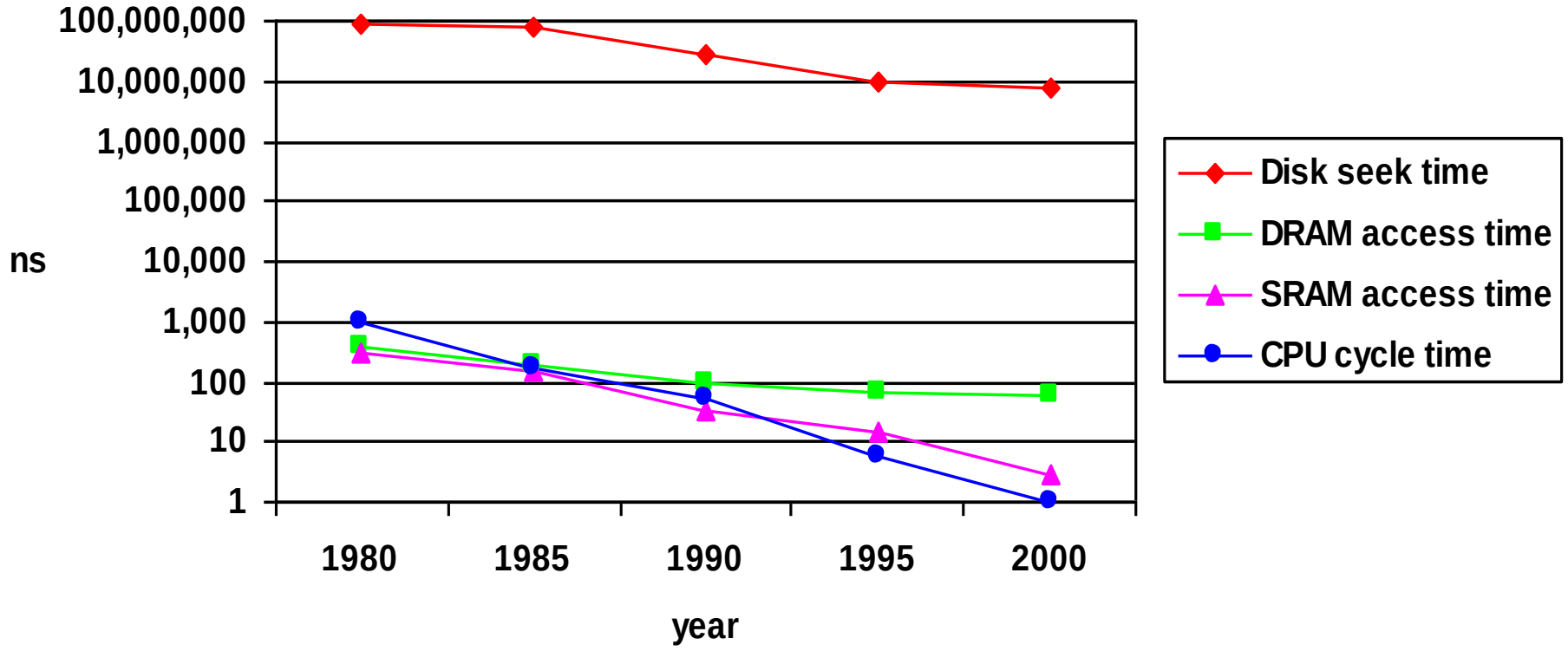
# Reading a Disk Sector (3)




When the DMA transfer completes, disk controller notifies CPU with *interrupt* (i.e., asserts special "interrupt" pin on CPU)

# The CPU-Memory Gap

- The increasing gap between DRAM, disk, and CPU speeds.



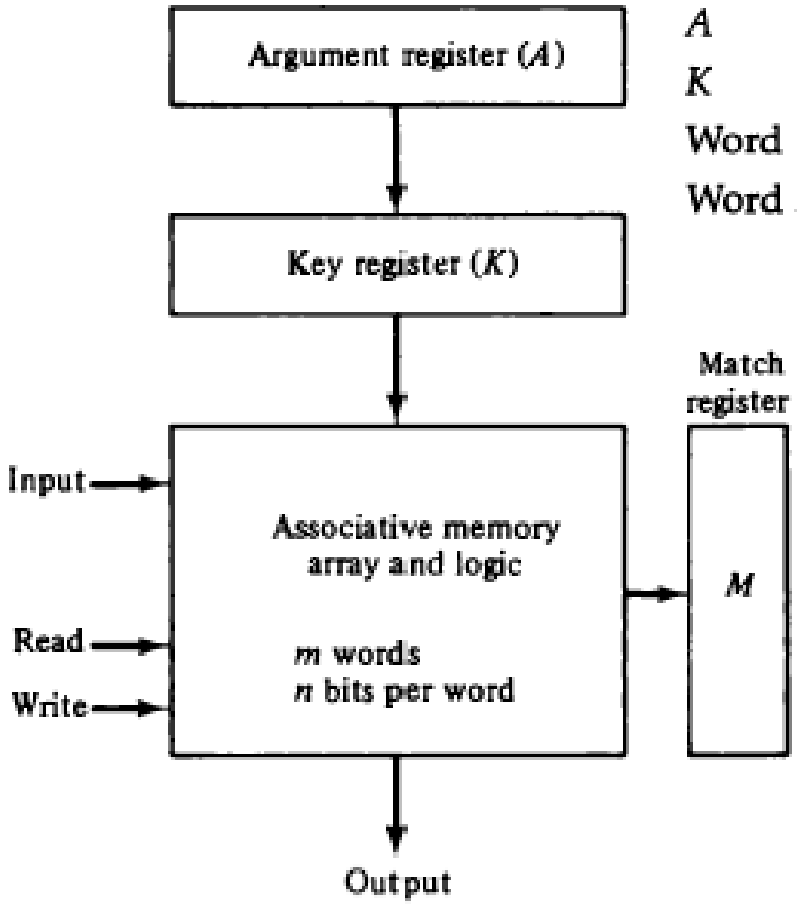
# Associative memory

- Memory access time is a crucial parameter with the performance point of view.
- The memory access time can be reduced considerably by,
  - Taking very fast memory devices
  - Decreasing the number of access to memory
    - Depends on location of content
    - Search algorithm
- Searching time required for an item can be reduced is data is accessed on the basis of content rather than the address of data itself.
- Memory unit addressable by its content is know as the content addressable memory (CAM)
- Entire memory is addressed simultaneously and in parallel format while on the basis of word contents.

# Associative memory cont….

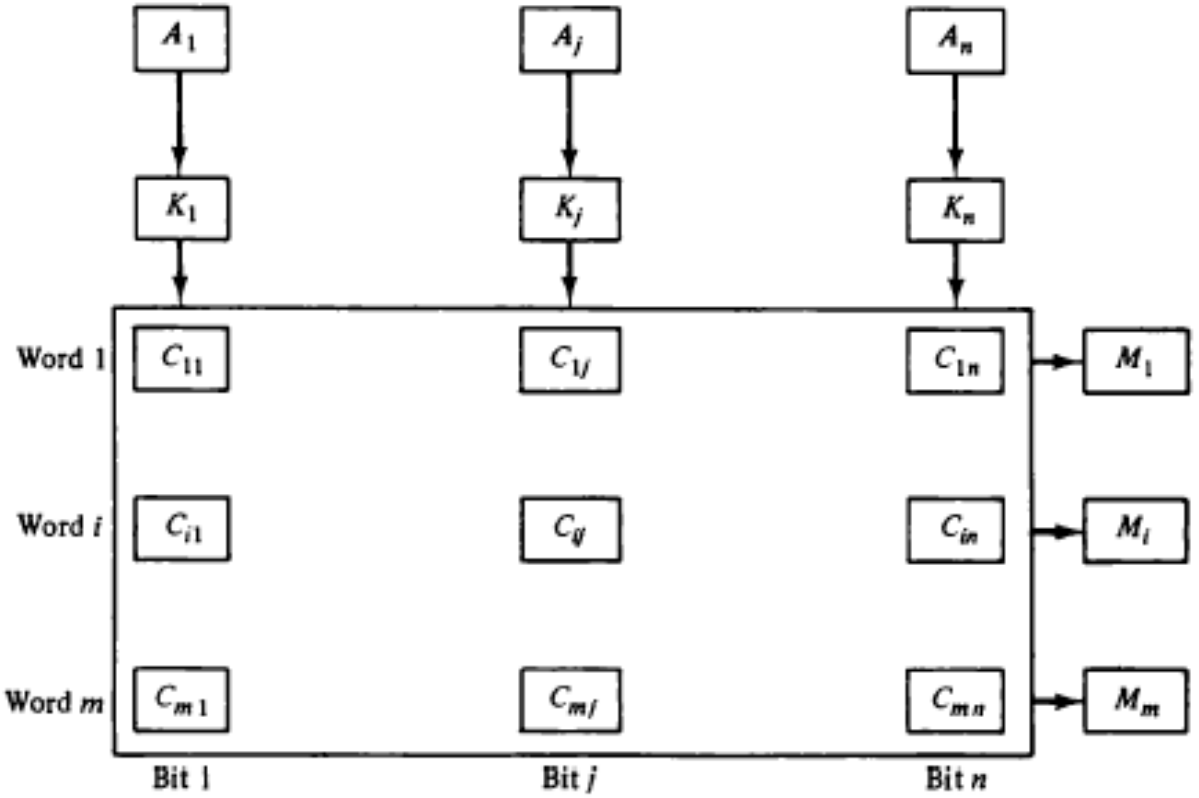
- No address is given while writing in CAM.
- Memory itself is capable of finding the unused / empty location to store a word.
- While reading the word from CAM a part of content of the word is specified,
- Memory locates all such matching words and mark them to be read.
- It is very costly because,
  - Each cell must have storage as well as matching logic capability.
- CAM are used only when the search time is very critical.

# HARDWARE ORGANIZATION FOR ASSOCIATIVE MEMORY




| | | |
|---|---|---|
| *A* | 101 111100 | |
| *K* | 111 000000 | |
| Word 1 | 100 111100 | no match |
| Word 2 | 101 000001 | match |

# Associative Memory with m-words and n-cells per word



# Associative memory cont....

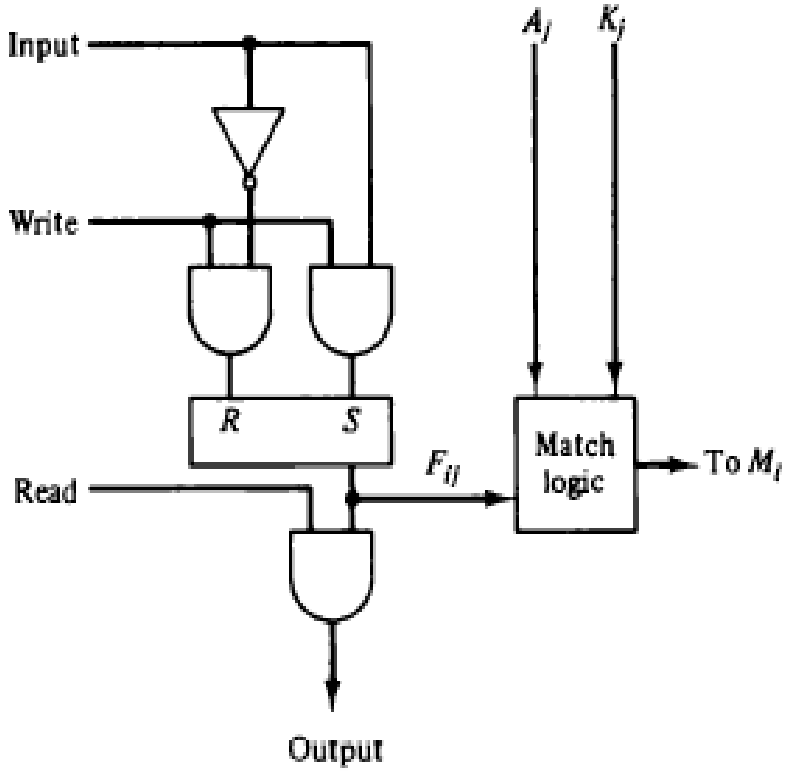
$$x_j = A_j F_{ij} + A_j' F_{ij}'$$

$$M_i = x_1 x_2 x_3 \cdots x_n$$

$$x_j + K_j' = \begin{cases} x_j & \text{if } K_j = 1 \\ 1 & \text{if } K_j = 0 \end{cases}$$

$$M_i = (x_1 + K_1')(x_2 + K_2')(x_3 + K_3') \cdots (x_n + K_n')$$

$$M_i = \prod_{j=1}^{n} (A_j F_{ij} + A_j' F_{ij}' + K_j')$$



# Read and write operations of associative memory

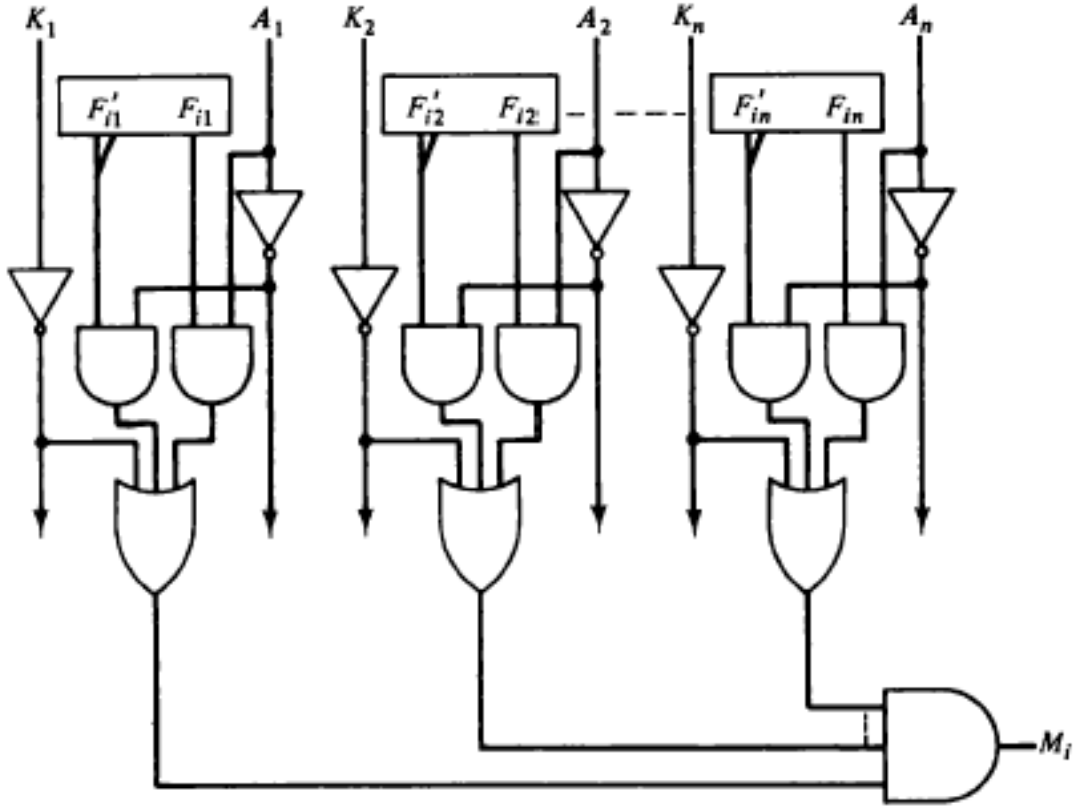



Figure 12-9 Match logic for one word of associative memory.

# Thank you