Computer Organization and Architecture

Under Graduate Course
(B. Tech-Information Technology, 2nd Semester)
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By

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Basics of Flip-flops and sequential circuits.

The output at any time instant is the function of only inputs at that time instant.

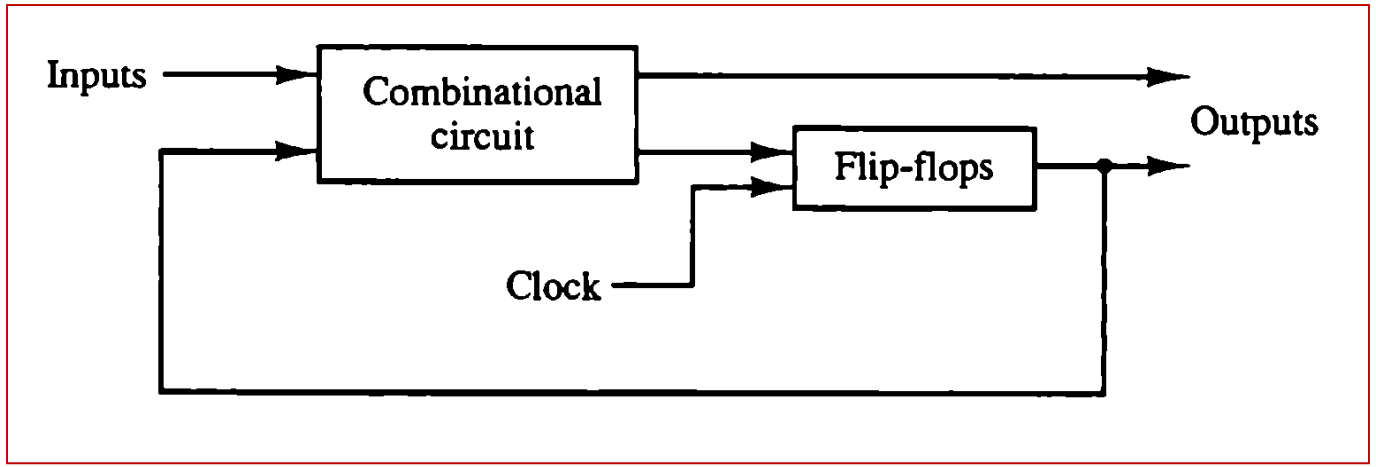
While in case of sequential circuits the out put at any instant of time is the function of inputs and some previous outputs also.

Basic building block for sequential circuit are latches/Flip-flops, which are generally known as the storage elements.

CONTI.....

Any sequential circuit consist of the following three sub-parts,

- Memory in feedback circuit
- Combinational circuit in forward circuit
- Clock signal for synchronization and control.



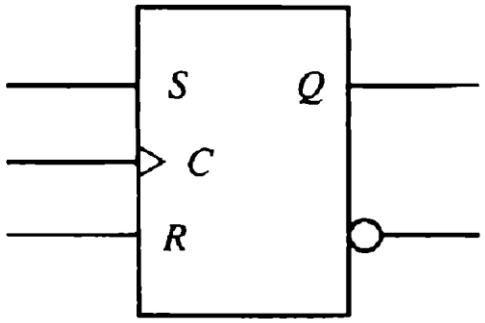
Synchronous and asynchronous digital circuits

The digital circuits in which the stages of all the storage elements changes simultaneously with the application of the common clock signal are known as synchronous sequential circuits.

Whereas the clock signal is applied generally on the first stage only and the output of the previous stage is used as the clock signal for subsequent stages.

The clock signal is rippled through all the subsequent stages in asynchronous circuits.

SR-FLIP-FLOP

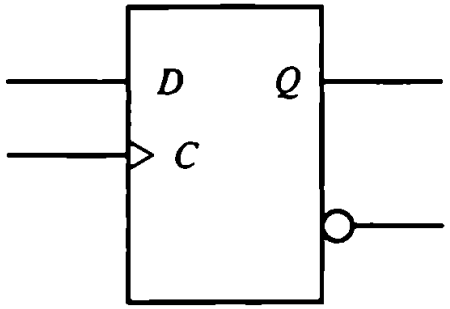


(a) Graphic symbol

S	R	Q (t + 1)	
0	0	Q (t)	No change
0	1	0	Clear to 0
1	0	1	Set to 1
1	1	?	Indeterminate

(b) Characteristic table

D-FF



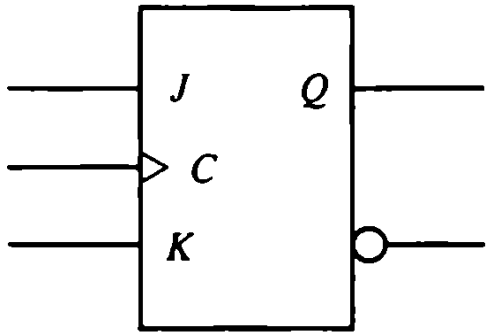
(a) Graphic symbol

D	Q (t + 1)	
0	0	Clear to 0
1	1	Set to 1

(b) Characteristic table

$$Q(t + 1) = D$$

JK-FF

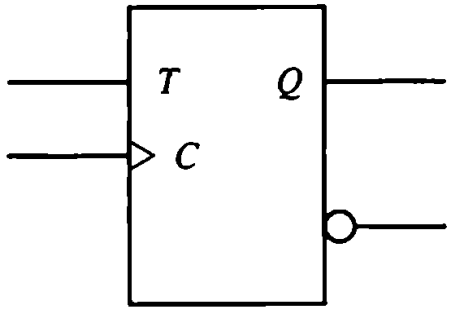


(a) Graphic symbol

J	K	Q (t + 1)	
0	0	Q (t)	No change
0	1	0	Clear to 0
1	0	1	Set to 1
1	1	Q′ (t)	Complement

(b) Characteristic table

T-FF



(a) Graphic symbol

T	$Q(t+1)$	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

(b) Characteristic table

$$Q(t+1) = Q(t) \oplus T$$

EXCITATION TABLES

SR flip-flop

$Q(t)$	$Q(t+1)$	S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

D flip-flop

$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

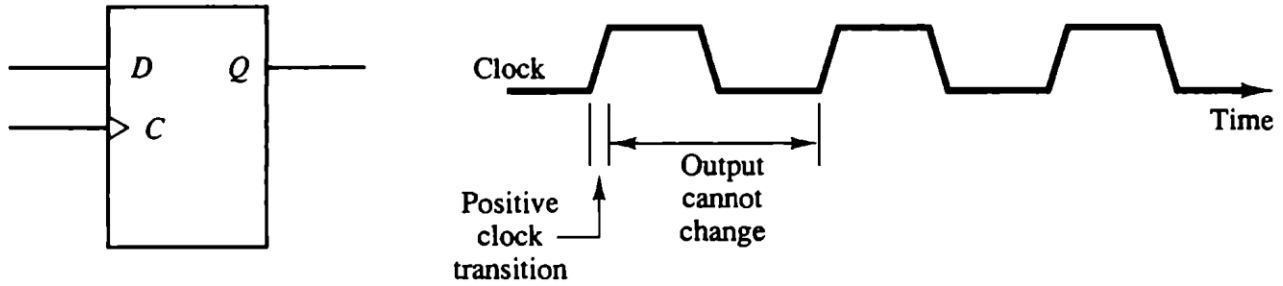
JK flip-flop

$Q(t)$	$Q(t+1)$	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

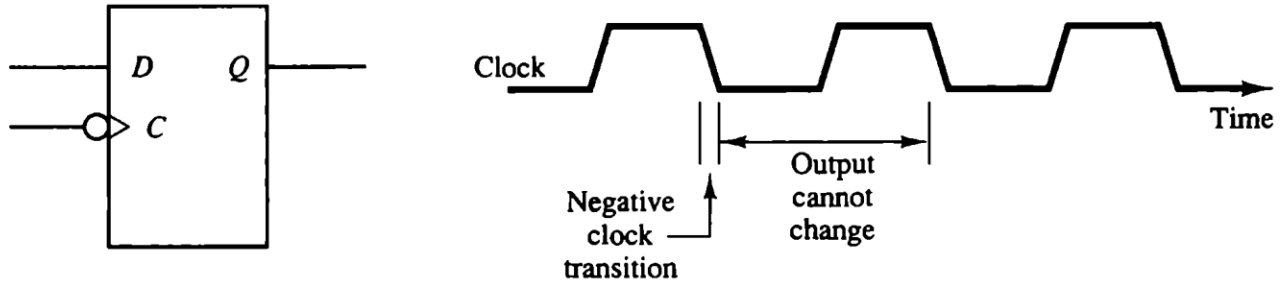
T flip-flop

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

Triggering of Flip-flops

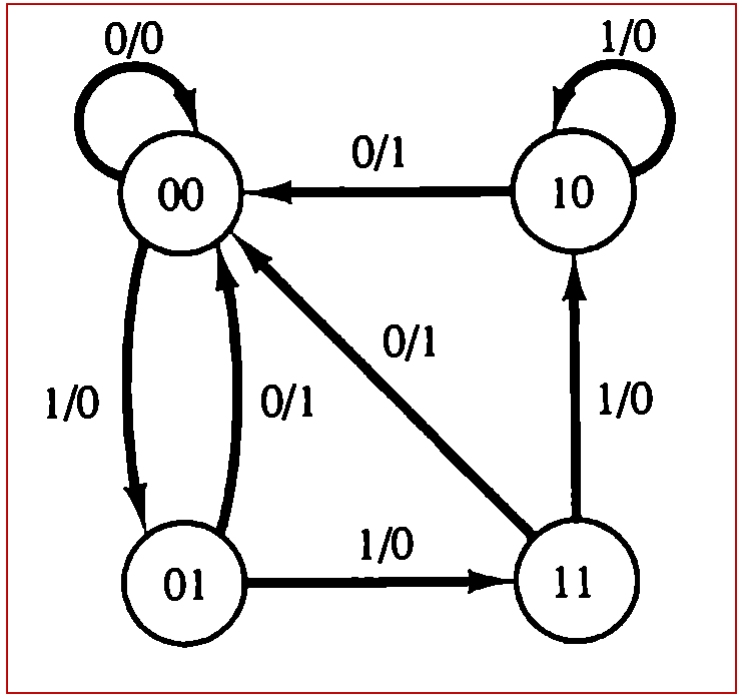


(a) Positive-edge-triggered *D* flip-flop.



(b) Negative-edge-triggered *D* flip-flop.

Sequential circuit design



CONTI….

Present state		Input	Next state		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

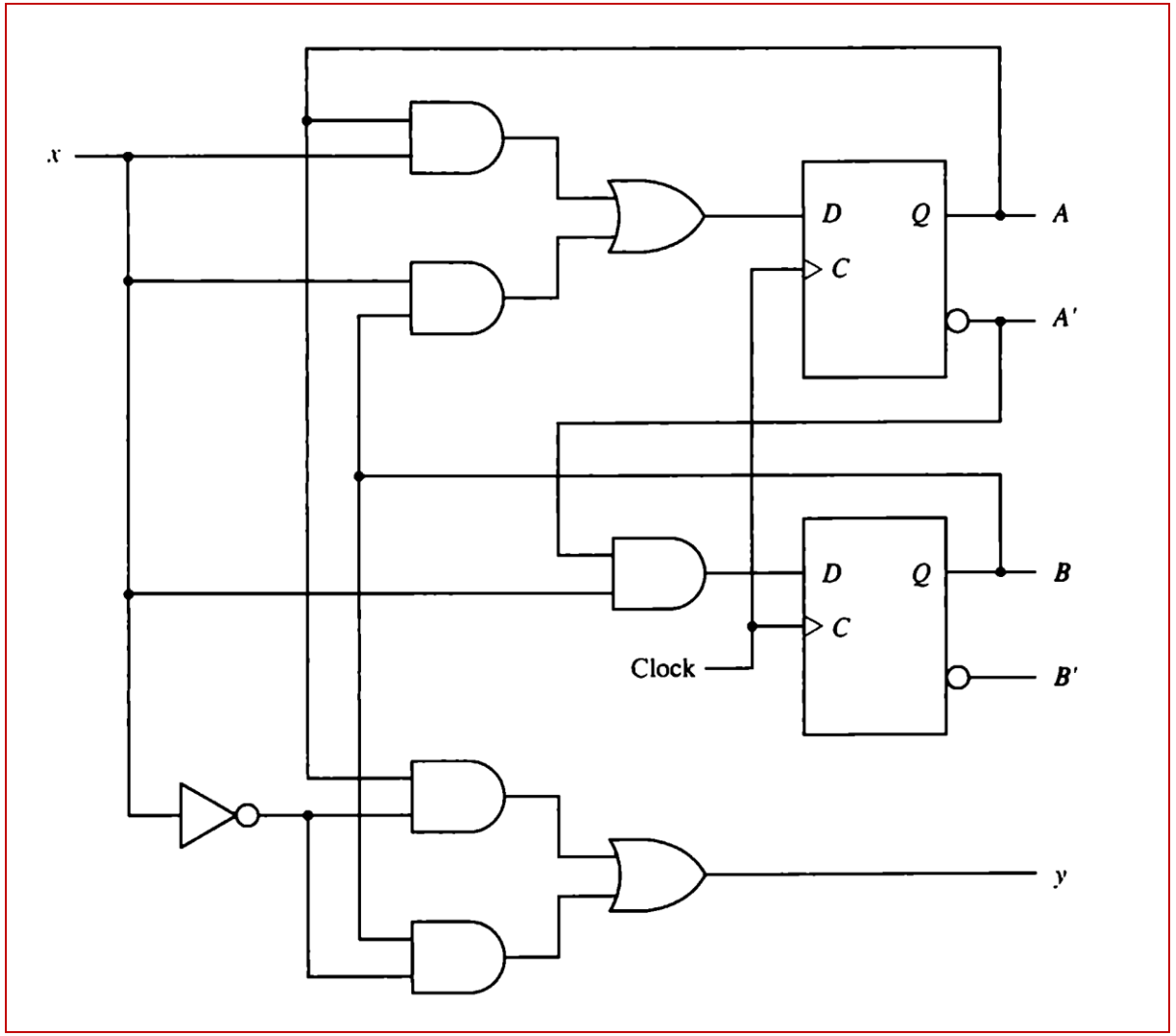
CONTI….

$$D_A = Ax + Bx$$

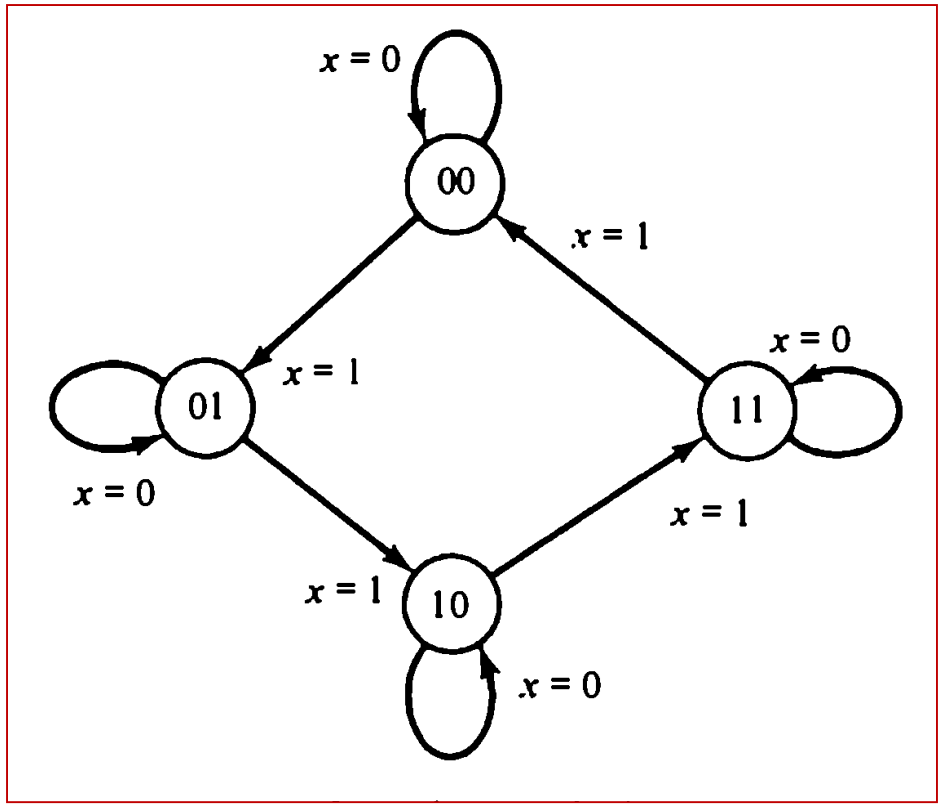
$$D_B = A'x$$

$$y = Ax' + Bx'$$

CONTI…



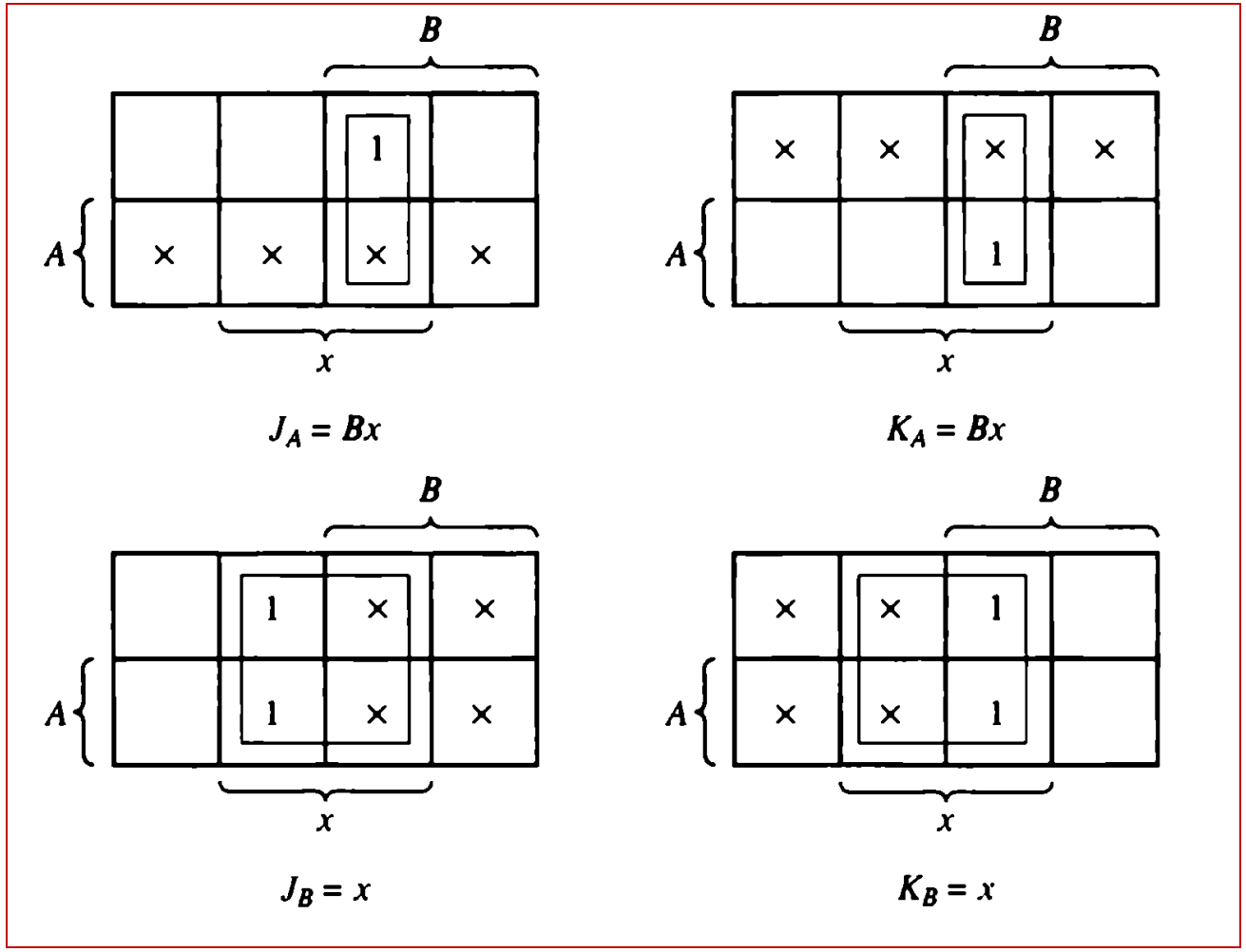
Design of a binary counter



EXCITATION TABLE FOR GIVEN PROBLEM

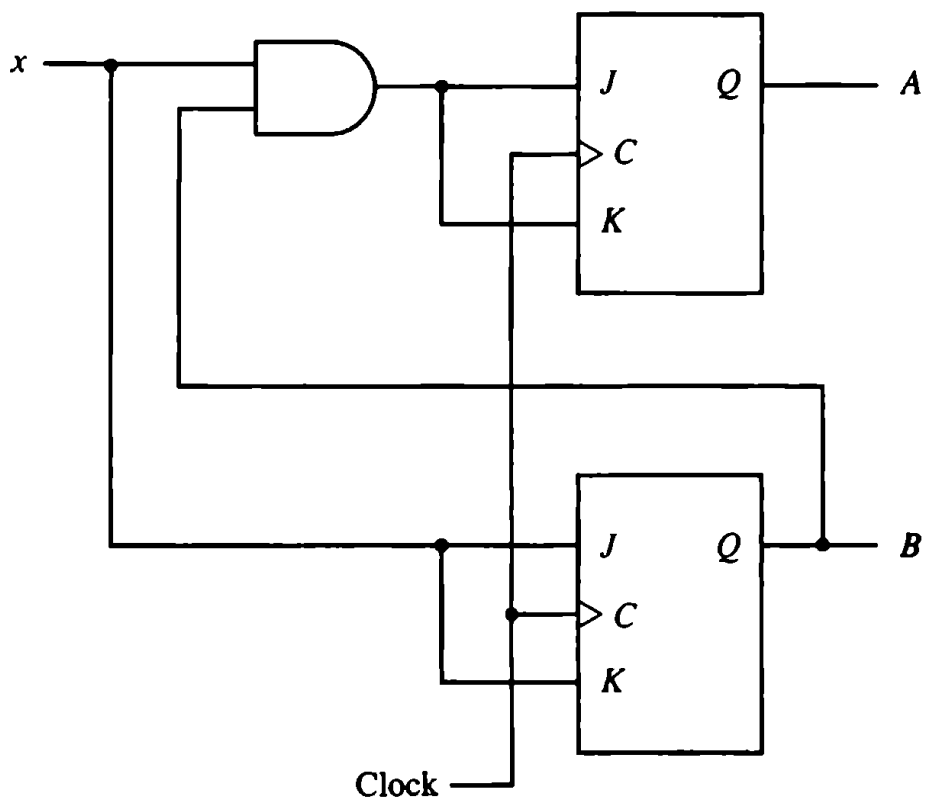
Present state		Input	Next state		Flip-flop inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	×	0	×
0	0	1	0	1	0	×	1	×
0	1	0	0	1	0	×	×	0
0	1	1	1	0	1	×	×	1
1	0	0	1	0	×	0	0	×
1	0	1	1	1	×	0	1	×
1	1	0	1	1	×	0	×	0
1	1	1	0	0	×	1	×	1

K-MAPS AND MINIMIZATION

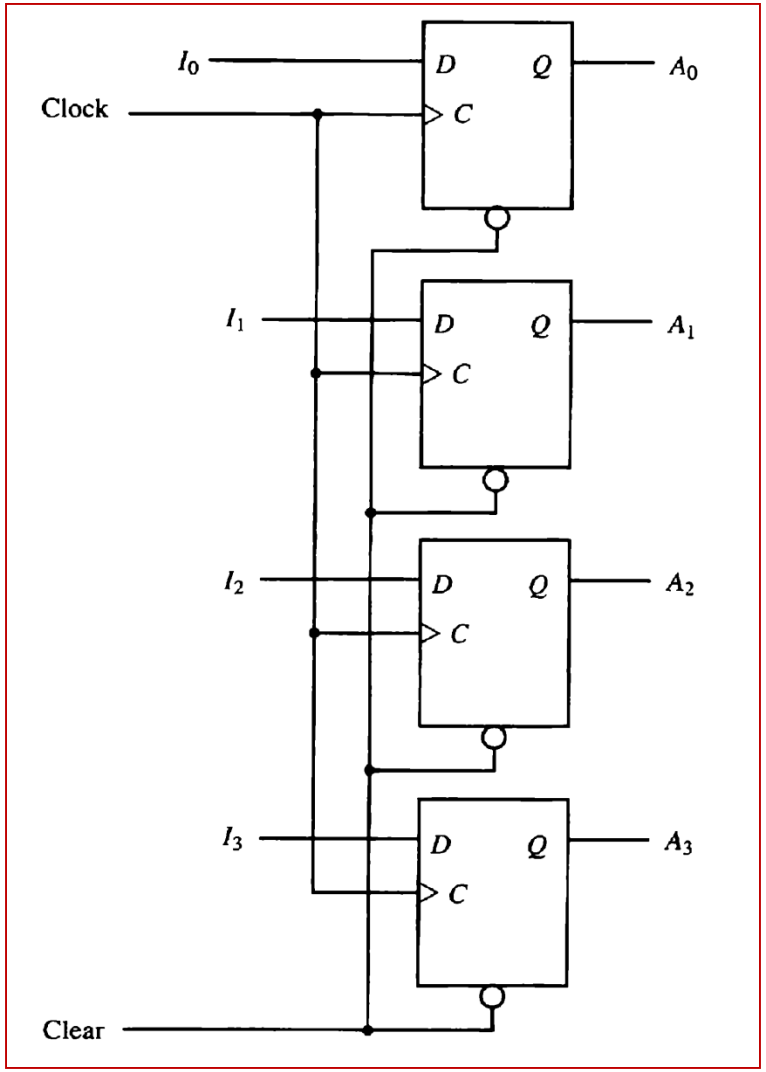


$J_A = Bx$ $K_A = Bx$

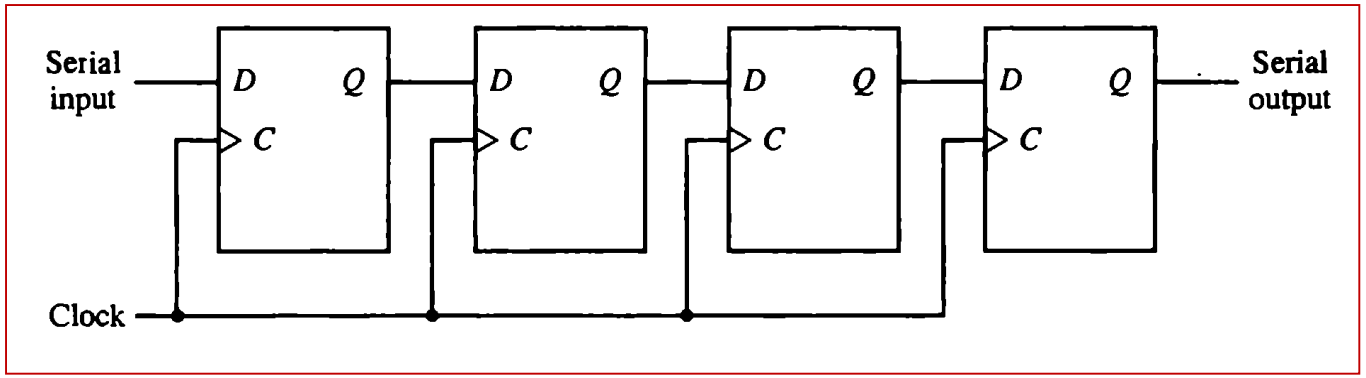
$J_B = x$ $K_B = x$



REGISTERS,

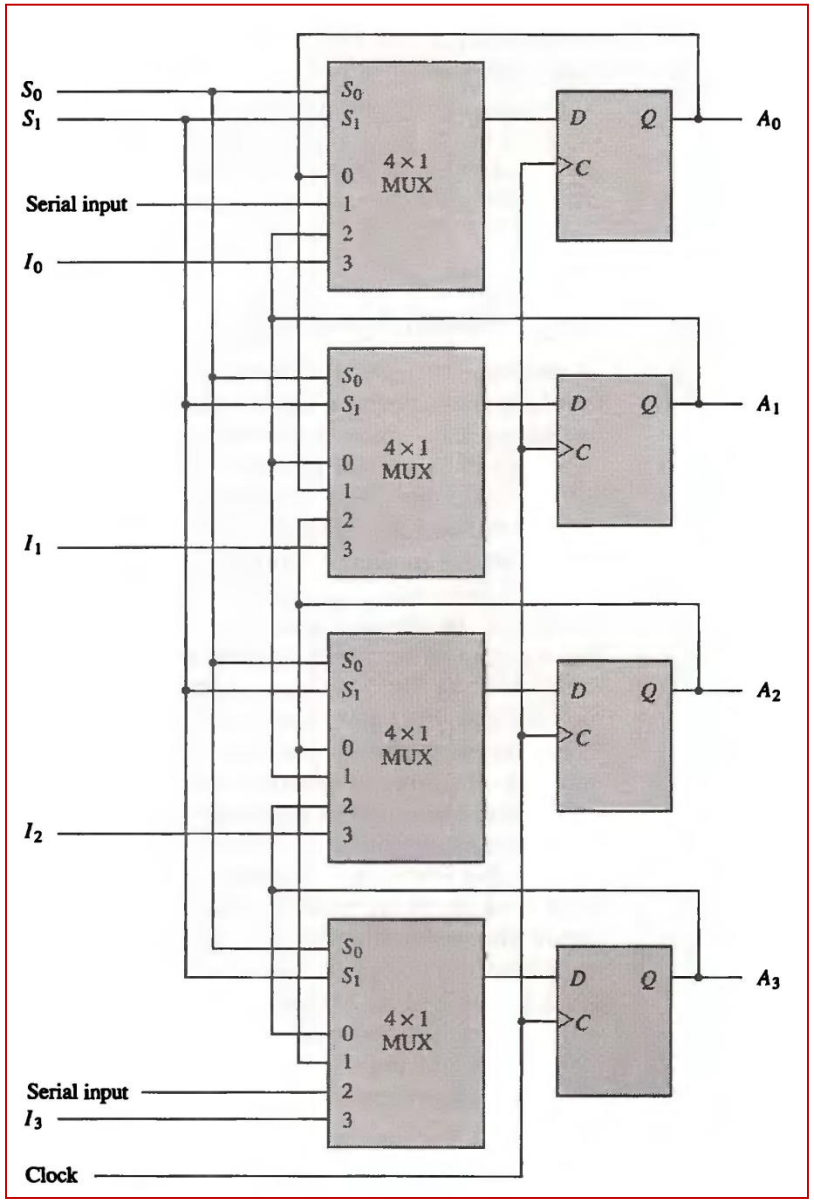


Shift Register (SISO)

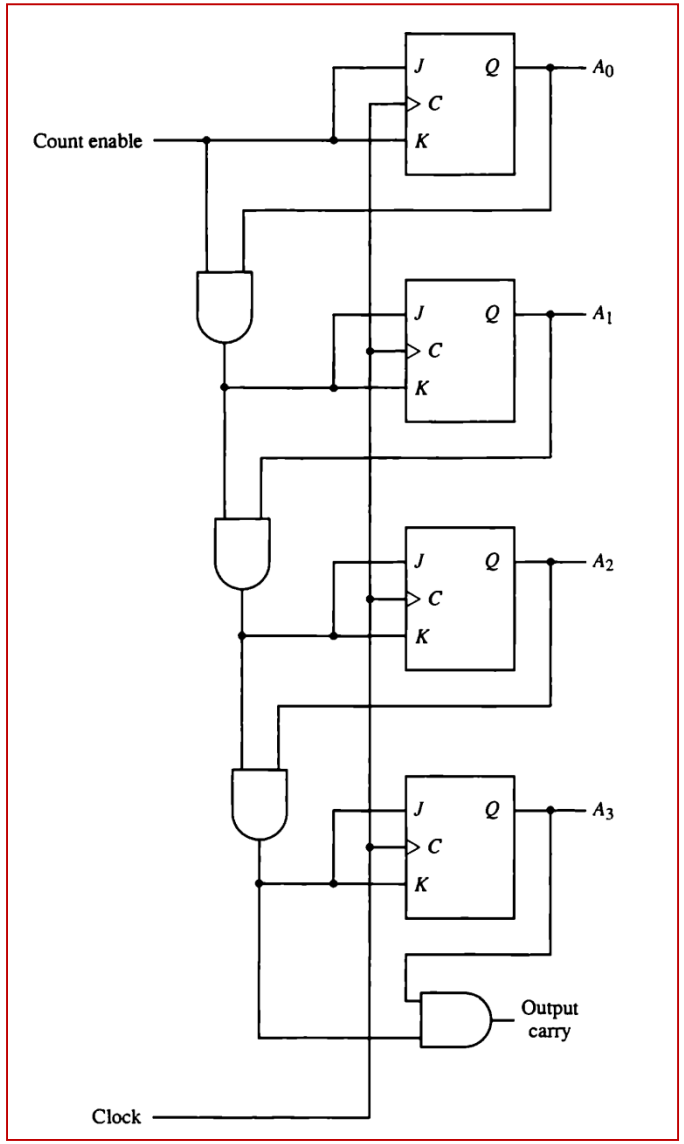


BIDIRECTIONAL SHIFT REGISTER

Mode control		
S_1	S_0	Register operation
0	0	No change
0	1	Shift right (down)
1	0	Shift left (up)
1	1	Parallel load

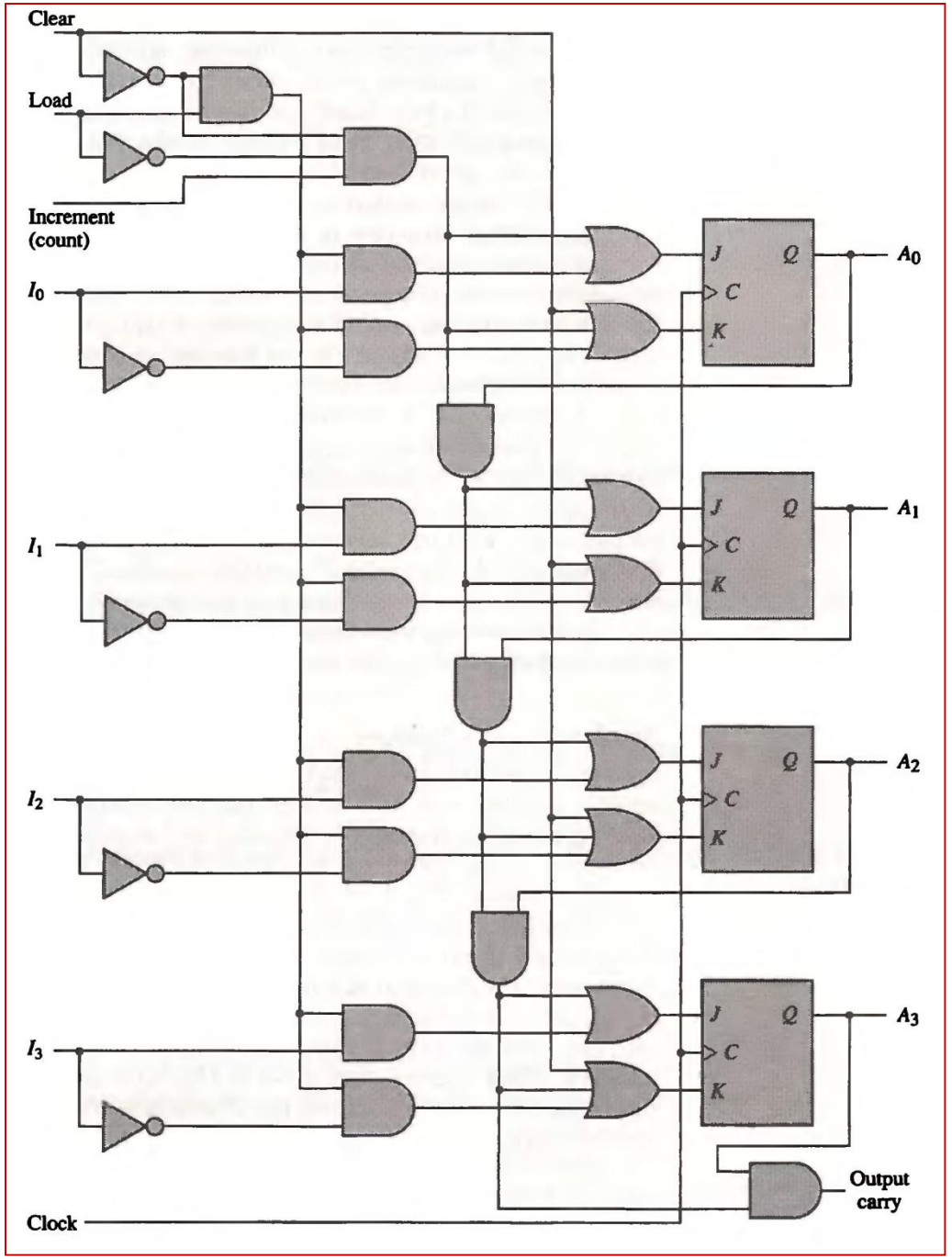


Binary counters (4-bit, Synchronous),



Binary counter with parallel load

Clock	Clear	Load	Increment	Operation
↑	0	0	0	No change
↑	0	0	1	Increment count by 1
↑	0	1	×	Load inputs I_0 through I_3
↑	1	×	×	Clear outputs to 0


Clear
Load
Increment
(count)
I_0
I_1
I_2
I_3
J
Q
C
K
A_0
A_1
A_2
A_3
Output
carry
Clock

Thank you