COMPUTER ARCHITECTURE AND ORGANIZATION TUTORIAL -01

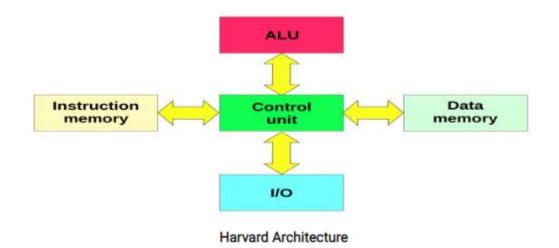
Dr. Satish Kumar Singh Associate Professor Indian Institute of Information Technology, Allahabad Email: sk.singh@iiita.ac.in

THE HARVARD ARCHITECTURE [AN OVERVIEW]

Key points-

- The Harvard architecture is nothing but a kind of storage of data. When it comes to the physical storage of the data the Harvard architecture always stood first.
- The main function of this architecture is to separate the physical storage of the data and give the single pathways for instruction and data.

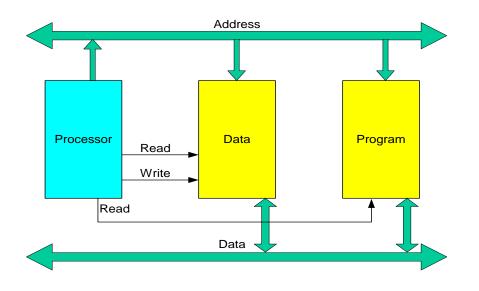
PICTORIAL REPRESENTATION



FEATURES OF THE HARVARD ARCHITECTURE

• Memory

- Separate memory into 2 types
 - Program memory
 - Data memory
- Used in MCS-51, MIPS etc.

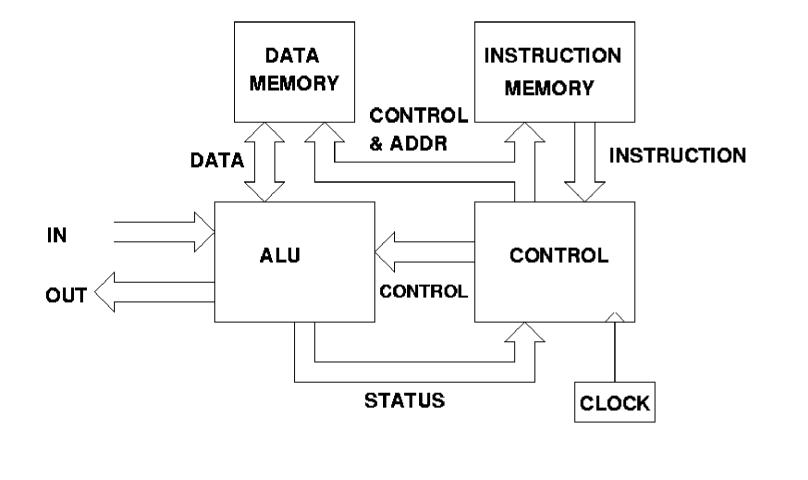


THE SPEED ASPECT

Key points

- The concept of the CPU cache is also being implemented
- Separate pathways for program and data memory respectively.

A DETAILED DESCRIPTION OF ARCHITECTURE



RISC AND CISC[AN OVERVIEW]

- The architecture of the Central Processing Unit (CPU) operates the capacity to function from "Instruction Set Architecture" to where it was designed.
- The architectural design of the CPU is
 - Reduced instruction set computing (RISC)
 - Complex instruction set computing (CISC)

REDUCED INSTRUCTION SET COMPUTING (RISC)

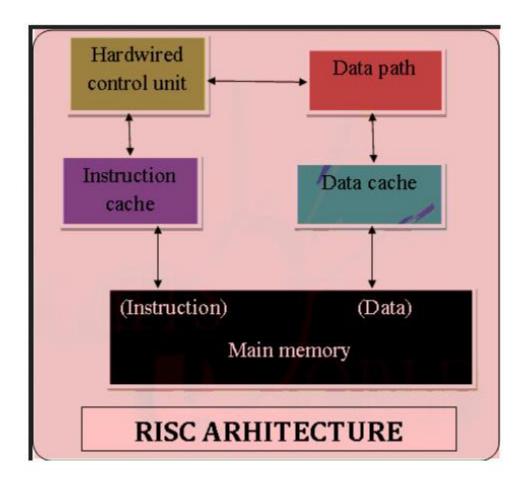
• It is a CPU design plan based on simple orders and acts fast.

- A reduced instruction set computer is a computer which only uses simple commands that can be divided into several instructions which achieve low-level operation within a single CLK cycle.
- In this machine, the instruction sets are modest and simple.
- Each instruction is about the similar length; these are wound together to get compound tasks done in a single operation

CONTD...

- Most commands are completed in one machine cycle.
 - This pipelining is a crucial technique used to speed up RISC machines.
- For example: **Suppose we have to add two 8-bit number.** Here programmer will write first load command to load data in registers then it will use suitable operator and then it will store result in desired location.

RISC ARCHITECTURE



SUMMARY RISC

- Simpler instruction, hence simple instruction decoding.
- Instruction come under size of one word.
- Instruction take single clock cycle to get executed.
- More number of general purpose register.
- Simple Addressing Modes.
- Less Data types.
- Pipeling can be achieved.

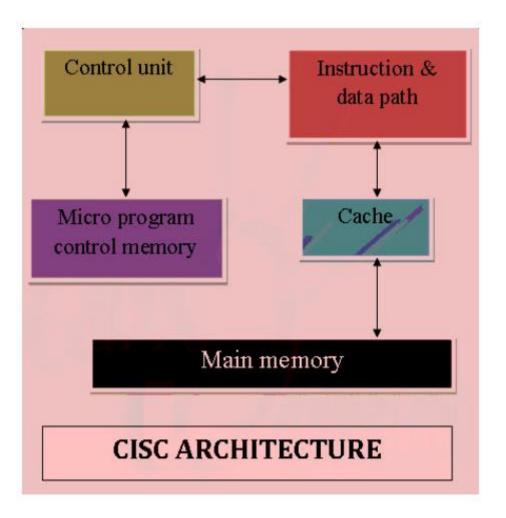
COMPLEX INSTRUCTION SET COMPUTING (CISC)

- It is a CPU design plan based on single commands, which are skilled in executing multi-step operations.
- It has a huge number of compound instructions, which takes a long time to perform.
- A complex instruction set computer is a computer where single instructions can perform numerous low-level operations.
 - load from memory,
 - an arithmetic operation,
 - a memory store

CONTD...

- Maximum instructions are finished in two to ten machine cycles.
 - In CISC, instruction pipelining is not easily implemented.
- For example: Suppose we have to add two 8-bit number: There will be a single command or instruction for this like ADD which will perform the task.

CISC ARCHITECTURE

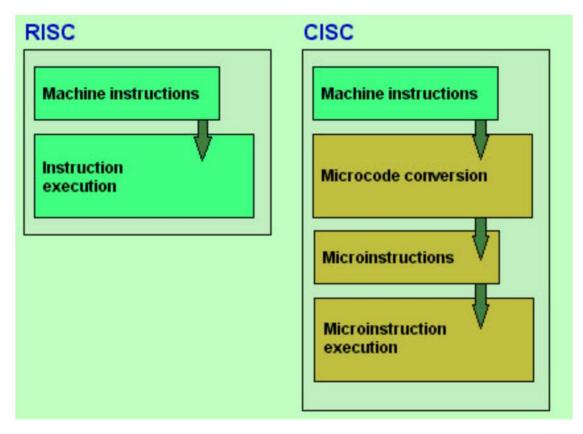




SUMMARY CISC

- Complex instruction, hence complex instruction decoding.
- Instruction are larger than one word size.
- Instruction may take more than single clock cycle to get executed.
- Less number of general purpose register as operation get performed in memory itself.
- Complex Addressing Modes.
- More Data types.

COMPARISON BETWEEN RISC AND CISC



- The RISC processors have a smaller set of instructions with few addressing nodes.
- The CISC processors have a larger set of instructions with many addressing nodes.

CONTD..

RISC	CISC
RISC has no memory unit and uses a separate hardware to implement instructions.	CISC has a memory unit to implement complex instructions.
RISC has a hard-wired unit of programming.	CISC has a microprogramming unit.
RISC is a complex compiler design.	CISC is an easy compiler design.
RISC calculations are faster and more precise.	CISC calculations are slow and precise.
RISC decoding of instructions is simple.	CISC decoding of instructions is complex.
Execution time is very less in RISC.	Execution time is very high in CISC.
Space is saved in RISC	In CISC space is wasted.

APPLICATIONS OF RISC AND CISC

• RISC is used in high-end applications.

- video processing,
- telecommunications
- image processing.
- CISC is used in low-end applications
 - security systems,
 - home automation, etc.

REFERENCES

- <u>http://www.ee.nmt.edu/~rison/ee308_spr00/supp/000119/harvard.</u> <u>gif</u>
- <u>https://www.listdifferences.com/difference-between-von-neumann-and-harvard-architecture/</u>
- <u>https://www.listdifferences.com/risc-and-cisc-architecture-their-differences/</u>