Computer Organization and Architecture Tutorial Session – 4
(Date – 04/02/2020)

1. What is the difference Between Byte addressable memory and Word addressable memorey?

Ans:

Byte Addressable	Word Addressable
When the ***data space in the cell = 8 bits*** then the corresponding ***address space*** is called as **Byte Address**.	When the ***data space in the cell = word length of CPU*** then the corresponding ***address space***is called as **Word Address**.
Based on this data storage i.e. *Bytewise storage*, the memory chip configuration is named as **Byte Addressable Memory**.	Based on this data storage i.e. *Wordwise storage*, the memory chip configuration is named as **Word Addressable Memory**.
For eg. : **64K X 8** chip has 16 bit Address and **cell size = 8 bits (1 Byte)** which means that in this chip, data is stored **byte by byte**.	For eg. : For a 16-bit CPU, **64K X 16** chip has 16 bit Address & **cell size = 16 bits (Word Length of CPU)** which means that in this chip, data is stored **word by word**

Memory Chip configuration having representation **'64 K x 8'**

1. Data Space in the Chip = 64K X 8
2. Data Space in the Cell = 8 bits
3. Address Space in the Chip =$\log_2$(64K) =16 bits

2. **How many address and data lines will be there for a 16M x 32 memory system?**

Ans

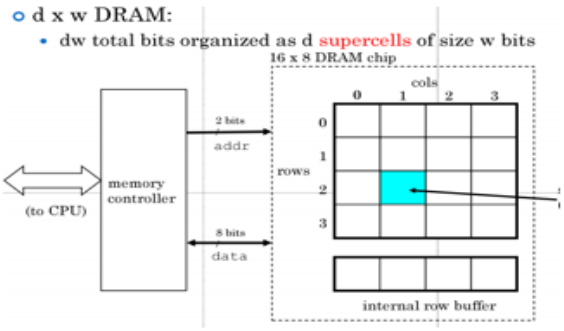
Since there are 16M words, the number of address lines will be 24, since 224 = 16M. Also since the word size is 32 bits, the number of data lines will also be 32

3. **Assume that a 1G x 1 DRAM memory cell array is organized as 1M rows and 1K columns. The number of address bits required to select a row and a column will be**

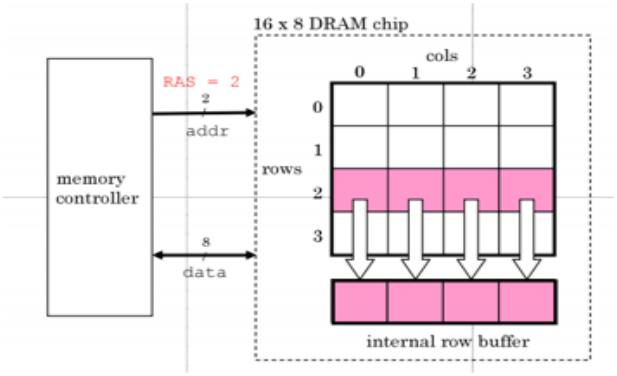
Ans :
Since there are 1M rows, the number of row address lines will be 20, as 220 = 1M. Also, for selecting one of the 1K columns, the number of column address lines will be 10, as 210 = 1K.

4. **How the row address strobe(RAS) and the column address strobe(CAS) helps in accessing a specific block of DRAM. Explain using an example with pictorial representation.**

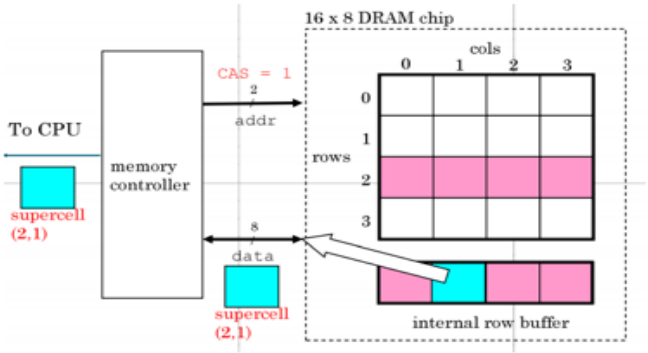
Ans- **Row address strobe -** RAS (row address strobe) is a signal sent to dynamic random access memory (DRAM) that tells it that an associated address is a row address. **Column address strobe-** Column address strobe is a signal sent to dynamic random access memory (DRAM) that tells it that an associated address is a column address.
A data bit in DRAM is stored in a cell located by the intersection of a column address and a row address.
Suppose we have to access data stored in a cell(2,1) Then Following steps are undertaken.



Supercell(2,1) needasto be copied



Row 2 is selected according to signal generated by RAS and the information is copied to internal row buffer from DRAM



Column 1 is selected according to signal generated by CAS and the selected cell(2,1) is copied to data line from internal row buffer and subsequently to CPU

5. **What is the bus? Explain its structure and topologies in reference to read and write operations.**

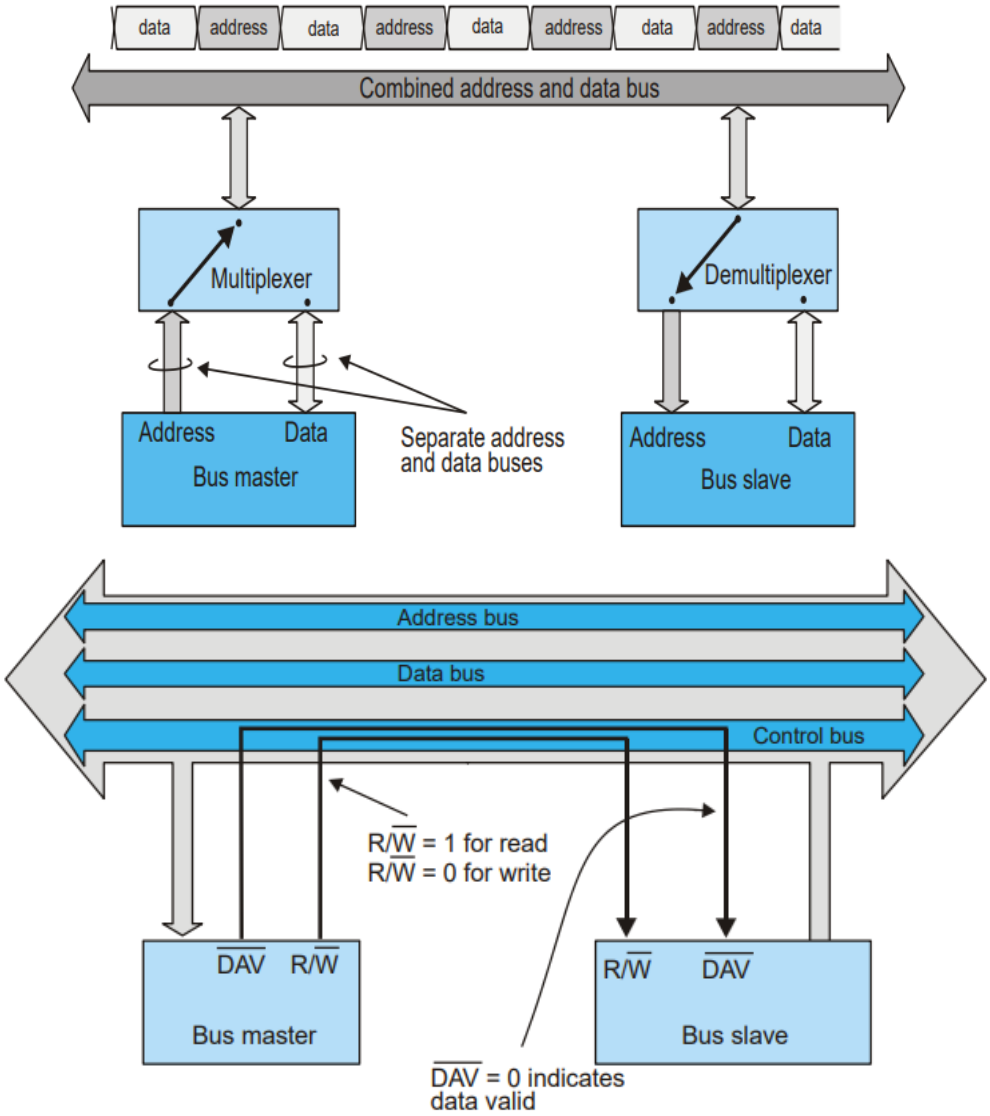
Ans- A group of electrical lines/wires that carry computer signals. A bus is a shared transmission medium Lines are assigned names for identification. Each carries a single electrical signal e.g. 1-bit memory address, a sequence of data bits, or timing control that turns a device on or off It possible to transfer data from one location in the computer system to another (between various I/O modules, memory and the CPU) Buses are notated on diagrams using widened lines or with a number to indicate the number of separate lines The bus is not only cable connection but also hardware (bus architecture), protocol, software, and bus controller.

Bus Structure and Topologies:-

Lines are grouped as follows

1. Power line provides electrical power to attached components
2. Data lines carrying the data or instructions between system modules
3. Address lines specify the recipient of data on the bus
4. Control lines provide control for the synchronization and operation of the bus and of the modules that are connected to the bus

It can be seen from the figure below, during a read cycle, data flows from the bus slave to the bus master and during a write cycle data flows from the master to the slave.



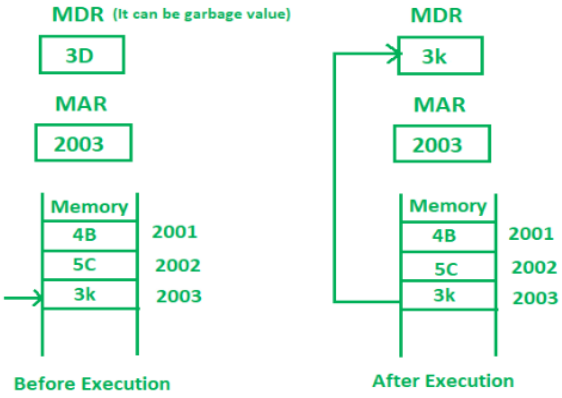
6. **Explain Memory Address Register and Memory Data Register in the context of memory r/w operations. Explain its relevance in read-write operation with proper pictorial representation.**

Ans- **Memory Address Register (MAR)** is the address register which is used to store the address of the memory location where the operation is being performed.

Memory Data Register (MDR) is the data register which is used to store the data on which the operation is being performed.

Memory Read Operation:

Memory read operation transfers the desired word to address lines and activates the read control line. Description of the memory read operation is given below:

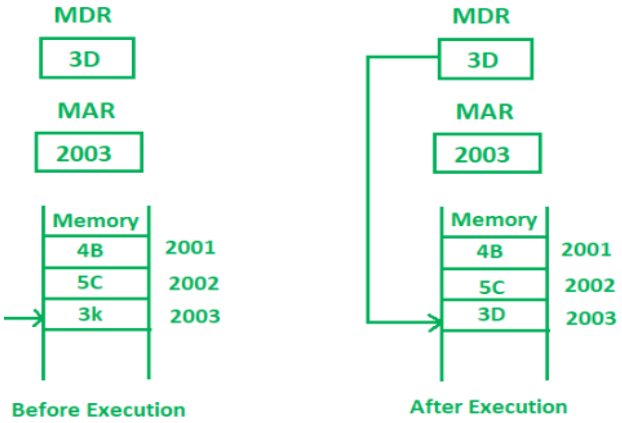


Memory Read Operation

In the above diagram initially, MDR can contain any garbage value and MAR is containing 2003 memory address. After the execution of read instruction, the data of memory location 2003 will be read and the MDR will get updated by the value of the 2003 memory location (3D).

Memory Write Operation:

Memory write operation transfers the address of the desired word to the address lines, transfers the data bits to be stored in memory to the data input lines. Then it activates the write control line. Description of the write operation is given below:

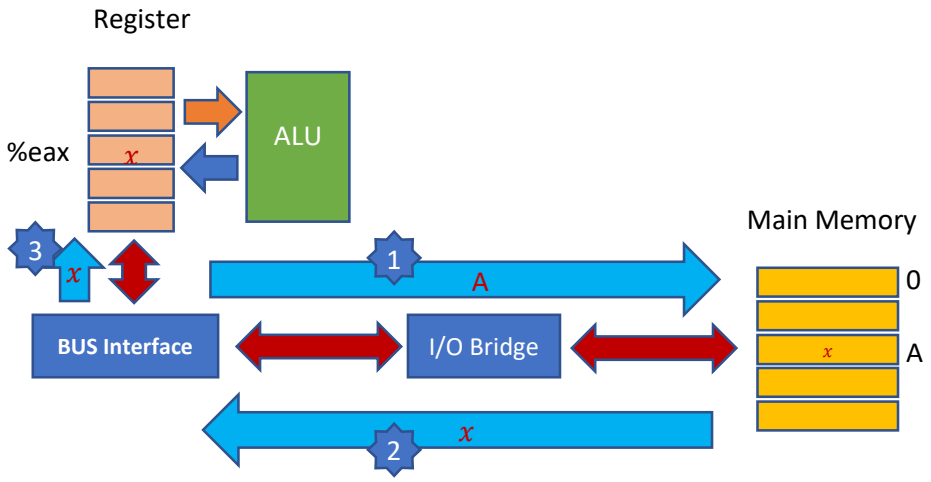


In the above diagram, the MAR contains 2003 and MDR contains 3D. After the execution of write instruction 3D will be written at 2003 memory location

7. What are the steps taken by CPU to read data from the memory? Explain with flow diagram for the instruction ***movl A, %eax***

For the instruction ***movl A, %eax***

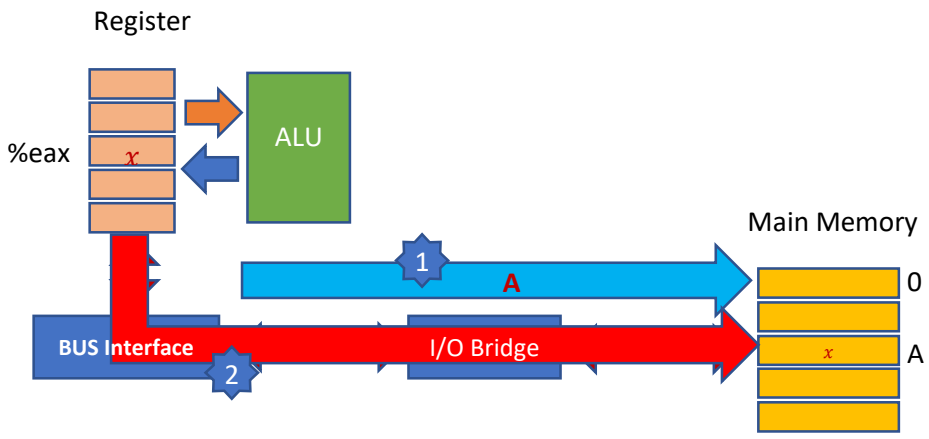
CPU places address **A** on the memory bus.
Main memory reads address A from the memory bus, retrieves the data (word x) and places it on bus.
CPU reads the data (word x) from bus and copies into register %eax.



8. What are the steps taken by CPU to write data to the memory? Explain with flow diagram for the instruction ***movl %eax, A***

For the instruction ***movl %eax, A***

a. CPU places address A on bus; main memory reads it and waits for corresponding data to arrive.
b. CPU places data word x on bus.
c. Main memory reads data word x from bus and stores it at address A.



9. Consider a hard disk with:
   4 surfaces
   64 tracks/surface
   128 sectors/track
   256 bytes/sector

   I. What is the capacity of the hard disk?
   II. The disk is rotating at 3600 RPM, what is the data transfer rate?
   III. The disk is rotating at 3600 RPM, what is the average access time?

Ans- i.)Disk capacity = surfaces * tracks/surface * sectors/track * bytes/sector
Disk capacity = 4 * 64 * 128 * 256
Disk capacity = 8 MB

ii)The disk is rotating at 3600 RPM, what is the data transfer rate?
60 sec -> 3600 rotations
1 sec -> 60 rotations
Data transfer rate = number of rotations per second * track capacity * number of surfaces (since 1 R-W head is used for each surface)
Data transfer rate = 60 * 128 * 256 * 4
Data transfer rate = 7.5 MB/sec

iii)Since seek time, controller time and the amount of data to be transferred is not given, we consider all the three terms as 0.
Therefore, Average Access time = Average rotational delay
Rotational latency => 60 sec -> 3600 rotations
1 sec -> 60 rotations
Rotational latency = (1/60) sec = 16.67 msec.
Average Rotational latency = (16.67)/2
= 8.33 msec.
Average Access time = 8.33 msec.

10. Consider a hard disk with 16 recording surfaces (0-15) having 16384 cylinders (0-16383) and each cylinder contains 64 sectors (0-63). Data storage capacity in each sector is 512 bytes. Data are organized cylinder-wise and the addressing format is . A file of size 42797 KB is stored in the disk and the starting disk location of the file is <1200, 9, 40>. What is the cylinder number of the last sector of the file, if it is stored in a contiguous manner?

Ans- File size is 42797KB= 42797*2^10B=85594*2^9B.
Now one sector=512B
so file will be stored in 85594 sectors i.e we need to cross 85594 sectors
starting of the file is
number of cylinders to cross=85594/16*64= 83 cylinders
remaining sectors to cross=85594-(83*16*64)=602
number of surfaces to cross=9
so to cross 9 surface we need to cross on more cylinder as file has started at surface 9 and no of surface in cylinder is 16 so
number of cylinder to cross=83+1=84
so cylinder no. 1200+84=1284

11. A hard disk system has the following parameters :

1. Number of tracks = 500
2. Number of sectors/track = 100
3. Number of bytes /sector = 500
4. Time taken by the head to move from one track to adjacent track = 1 ms
5. Rotation speed = 600 rpm.

What is the average time taken for transferring 250 bytes from the disk?

Ans- **Avg. time to transfer = Avg. seek time + Avg. rotational delay + Data transfer time**

- **Avg Seek Time** – time taken to move from 1st track to 1st track : 0ms, 1st to 2nd : 1ms, 2ms, 3ms,….499ms
  Avg Seek time =(**Σ**0+1+2+3+…+499)/500 = 249.5 ms

- **Avg Rotational Delay –** RMP : 600 , 600 rotations in 60 sec (one Rotation = 60/600 sec = 0.1 sec) So, Avg Rotational Delay = 0.1/2= 50 ms

- **Data Transfer Time:** In 1 Rotation we can read data on one track = 100 * 500 = 50,000 B data is read in one rotation. 250 bytes -> 0.1 * 250 / 50,000 = 0.5 ms

Therefore ATT = 249.5+50+0.5 = 300 ms

12. **MCQs:**

- What is used for writing/reading of data to/from a magnetic ribbon???
  - Magnetic tape
- The disk's surface is divided into a number of invisible concentric circles called:
  - Tracks
- How many bytes in a sector in general?
  - Each track of a disc is divided into sectors. A sector typically contains 512 bytes. Disk drives are designed to read/write only whole sectors at a time.
- Disk access time does not depends on which of the following factors
  - Seek time
  - Latency
  - Transfer rate
  - Arrival rate

  Ans is: Arrival rate

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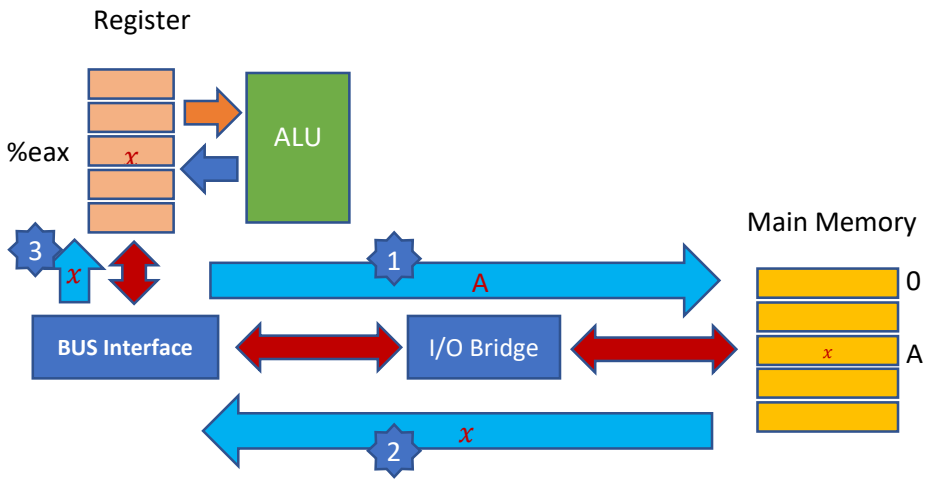

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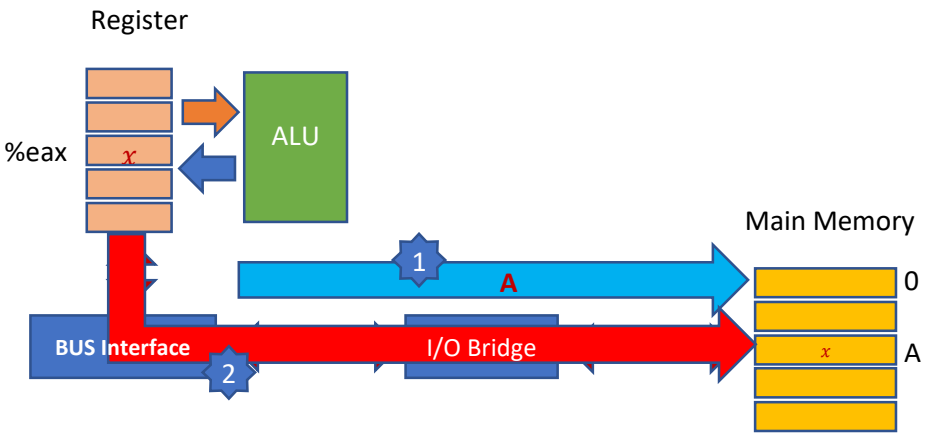


15. **Among sequential access, direct access, and random access, which one is fastest? Why?**

Random Access.

Sequential Access: Memory is organized into units of data called records. Access must be made in a specific linear sequence.

Direct Access: Individual blocks or records have a unique address based on physical location. Access is accomplished by direct access to reach general vicinity plus sequential searching, counting, or waiting to reach final location.

Random Access: Each addressable location in memory has a unique, physically wired-in addressing mechanism. The time to access a given location is independent of the sequence of prior accesses and is constant.

16. **What is the general relationship among access time, memory cost, and capacity?**

Faster access time, greater cost per bit; smaller capacity,

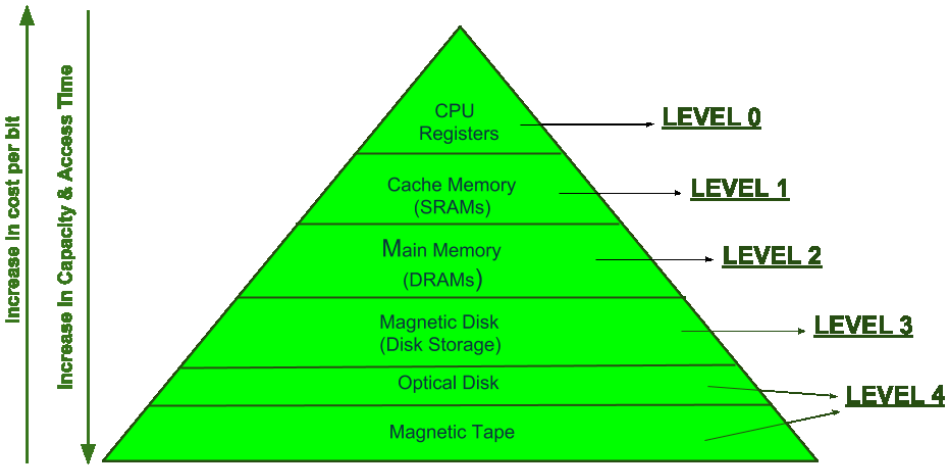
smaller cost per bit; greater capacity, slower access time.

17. **List the characteristics of memory in terms of performance. Explain the meaning of each characteristic.**

OR

Explain the Memory hierarchy design and its characteristics.

In the Computer System Design, Memory Hierarchy is an enhancement to organize the memory such that it can minimize the access time. The Memory Hierarchy was developed based on a program behavior known as locality of references.The figure below clearly demonstrates the different levels of memory hierarchy:



MEMORY HIERARCHY DESIGN

This Memory Hierarchy Design is divided into 2 main types:

External Memory or Secondary Memory –
Comprising of Magnetic Disk, Optical Disk, Magnetic Tape etc. that is peripheral storage devices which are accessible by the processor via I/O Module.
Internal Memory or Primary Memory –
Comprising of Main Memory, Cache Memory & CPU registers. This is directly accessible by the processor.

We can infer the following characteristics of Memory Hierarchy Design from above figure:

Capacity:
It is the global volume of information the memory can store. As we move from top to bottom in the Hierarchy, the capacity increases.
Access Time:
It is the time interval between the read/write request and the availability of the data. As we move from top to bottom in the Hierarchy, the access time increases.
Performance:
Earlier when the computer system was designed without Memory Hierarchy design, the speed gap increases between the CPU registers and Main Memory due to large difference in access time. This results in lower performance of the system and thus, enhancement was required. This enhancement was made in the form of Memory Hierarchy Design because of which the performance of the system increases. One of the most significant ways to increase system performance is minimizing how far down the memory hierarchy one has to go to manipulate data.
Cost per bit: As we move from bottom to top in the Hierarchy, the cost per bit increases i.e. Internal Memory is costlier than External Memory.

18. **Write the difference between Random Access Memory and Content Addressable Memory.**

RAM:
Random Access Memory (RAM) is used to read and write. It is the part of primary memory and used in order to store running applications (programs) and program's data for performing operation. It is mainly of two types: Dynamic RAM (or DRAM) and Static RAM (or SRAM).

CAM:
Content Addressable Memory (CAM) is also known as Associative Memory, in which the user supplies data word and associative memory searches its entire memory and if the data word is found, It returns the list of addresses where that data word was located.

The difference table is given below on the basis of their properties:

S.NO	RAM MEMORY	ASSOCIATIVE MEMORY(CAM)
1.	RAM stands for Random Access Memory.	It stands for Content Addressable Memory.
2.	In RAM, the user supplies a memory address and RAM returns data word stored at the address.	In associative memory, the user supplies data word and associative memory searches its entire memory.
3.	The price of RAM is low as compared to Associative memory.	It is expensive than RAM.
4.	It is used to store running applications(programs) and program's data for performing operation.	It is widely used in database management system.
5.	This is suitable for algorithm based search via PRAM. PRAM stands for Parallel-RAM.	This is suitable for parallel search.
6.	If the data word is found, RAM returns the data word.	If the data word is found, It returns the list of addresses where that data word was located.

19. **Give methods to reduce memory access time:**

The two basic ways of ensuring this are:

- Reducing the number of access to memory via:
  - Checking for location of content
  - Using specialized algorithms
- Using very fast memory access devices

20. **Define Content Addressable Memory (CAM). When is it used? Why is it generally not used?**

When memory unit is addressed directly by the content it has, it is known as CAM.

CAM is very fast because the entire memory is read at a time, all matching cases are found and all the locations are simultaneously read. Thus. It is used when the primary optimization parameter is the search time.

CAM is very costly because each memory cell must simultaneously be capable of storage as well as information matching logic.

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